iND83209
Datasheet
Rev 1.7

1 REVISION HISTORY

Table 1 Revision History

Rev #	Date	Action	By
0.7	10/14/2020	First Release.	JackZhu
0.8	06/03/2021	LIN Master Description updated: 1. Added a limitation that LIN Master only supports auto-baudrate LIN Slave.	JackZhu
0.9	08/05/2021	Updated the package	Hebe
1.0	08/15/2021	Updated the register map description by adding the configuration of glitch-filter function	FlavinLi
1.1	02/17/2022	Updated the Table 15 Tempsensor Output voltage vs Junction Temp	Hebe
1.2	03/22/2022	Updated the Figure 6 Clock Generation	Flavinli
1.3	06/15/2022	Added power on sequence	Hebe
1.4	10/27/2022	Updated the figure6 and figure7 in 9.2.1 power on sequence	Flavinli
1.5	11/25/2022	Updated the regmap	Hebe
1.6	9/18/2023	1. Updated spec. of bandgap voltage 2. Updated style of pinout diagram 3. Added MSL level of package	Daniel
1.7	10/27/2023	Updated the description of 8.2.18.11 TRIM	Flavinli

2 TABLE OF CONTENTS

3 LIST OF TABLES

4 LIST OF FIGURES

Figure of Contents

5 ORDERING INFORMATION

Part number	Package	MSL	Shipping
iND83209	QFN20	Level 1	4000pcs/Tape&Reel

6 SYSTEM OVERVIEW

"iND83209" IC is an automotive LED lighting integrated device that combines together a 32bit MCU (Cortex M0) with a power management unit capable of handling 45V Load dump from the car battery, 3 high voltage constant current open drain IO with PWM, a LIN slave transceiver supporting LIN auto-addressing, a LIN master transceiver for extension and an integrated 10 bit ADC for monitoring, aging and temperature compensation purpose.

- Full automotive qualification AEC-Q100 Grade1
- Functional Safety Enhancements:
    - Two independent hardware LIN TX monitors for LINS/LINM to prevent a dominant bus caused by internal malfunction.
    - LIN Bus Idle timeout monitors
        - Always active, even the chip is in hibernate mode.
        - For preventing a fast discharge of the car battery, if a short to ground is detected, the following options are available:
            - Automatically switch off LIN slave's pullup.
            - Reduce LIN master's pullup from 1K to 30K.
            - Disable lin switch automatically.
        - Auto-recovery if the failure condition disappears.
- CPU architecture:
    - ARM Cortex M0 processor
    - System Tick Timer (Systick, 24bits, interruptible)
    - Serial Wire Debugger (ARM)
    - Built-in Nested Vectored Interrupt Controller (NVIC)
    - Programmable Watch-Dog Timer
    - 3 programmable timers
- Memory:
    - 64kBytes of Flash Program Memory, 10 years retention in automotive environment
    - 16kBytes of SRAM
- Peripherals/Digital Features
    - Clock and Reset Manager

- Two internal clock resources:
  - Trimmable Auxiliary ROSC with two modes:
    - 256KHz mode which supports more flexible/accurate LIN wakeup filtering. Auxiliary system clock frequency is 256KHz/16.
    - 32KHz mode(default). Auxiliary system clock frequency is 32KHz/2.
  - Trimmable 8~16MHz ROSC with SSC support
- Reset Sources:
  - POR and BOR (no external reset)
  - SW Triggers: Hard/Soft

- Power Management
  - Active Mode
  - CPU Sleep Mode
    - Triggered by Cortex-M0 WFI instruction
    - Wakeup Resources: Interrupts/Exceptions
  - Hibernate Mode (ASIC always-on/MCU power-off)
    - Wakeup Resources: GPIOs/LINS/LINM/Wakeup Timer
- One SAE J2602/LIN2.2 LIN Slave Controller and Transceiver
  - Supports LIN auto-addressing through an internal LIN switch.
- One LIN Master Controller and Transceiver
  - Only available when the internal LIN switch is not used.
  - Only supports auto-baudrate LIN Slaves.
- Watch dog timer (ASIC side) with window mode support
- 3x16bits PWM required to control LED current driver:
  - Common prescaler and 16bit timer
  - Support power balance with independent rise/fall timing configuration
- General Purpose IOs x 6：
  - Dual edges detection interrupt supported
  - PWM mode supported
  - External LIN Transceiver interconnection capability

- LINM RxD/TxD: GPIO1/GPIO2
- LINS RxD/TxD: GPIO3/GPIO4 or GPIO5/GPIO6

- Peripherals/Analog Features:
  - 3 Programmable 60mA max constant current / high voltage IO open drain
  - PN voltage measurement for temp compensation:
    - Integrated a dedicated 2.5mA current source
    - Fully differential measurement
  - Temperature Sensor/Monitor with ADC
  - Battery voltage detection and monitoring
  - Hardware over temperature protection
  - 10 bits SAR ADC with 13 channels
    - Buffered bandgap voltage
    - Junction Temperature
    - Forward voltages of 3 external LEDs
    - GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6
    - One accurate VBAT channel
    - MCU Core Voltage
  - Integrated voltage regulators
    - LDO 3.3Vout (ASIC Core and IO supply + MCU I/O)
    - LDO 1.5VOut (MCU Core/Flash)

6.1 APPLICATION BLOCK DIAGRAM

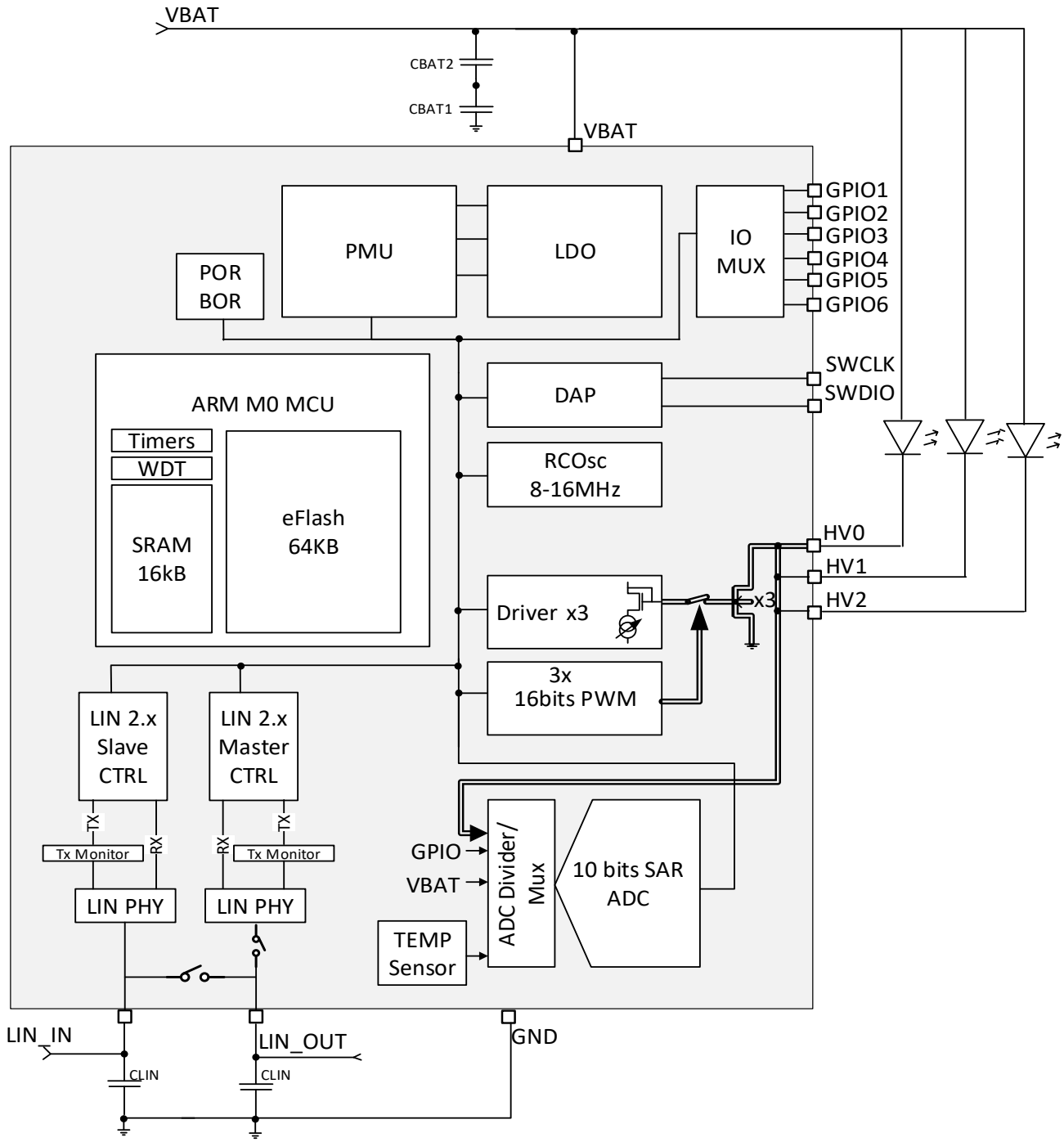


Figure 1 IC block diagram with external components

Note: The application block diagram does not include components used to qualify the system against ISO7637-2/-3.

6.2 PACKAGE OVERVIEW AND PIN DESCRIPTION

6.2.1 Package Outline

QFN20, 4x4 mm body size, 0.5 mm lead pitch.

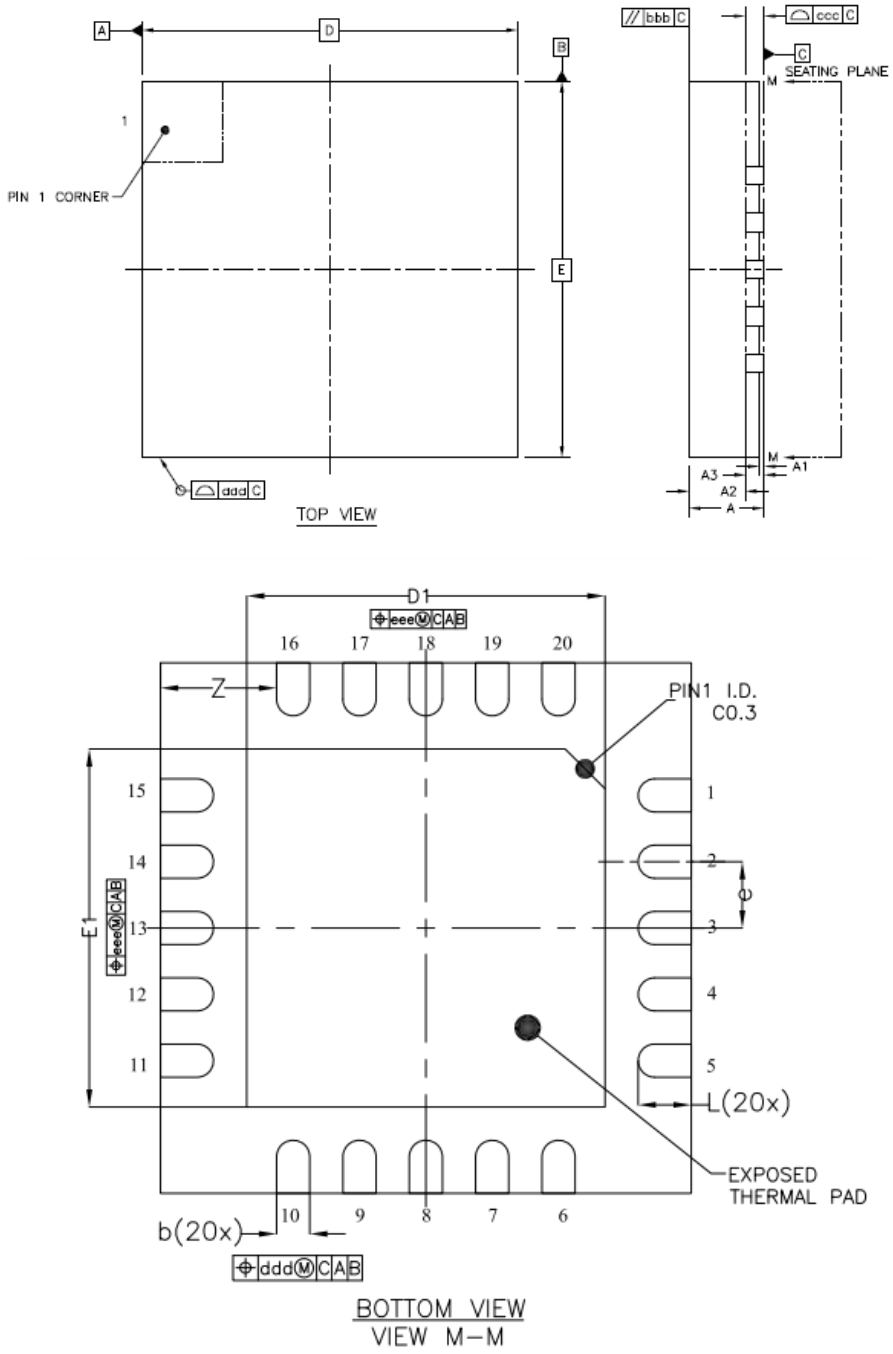


Figure 2 Package Outline

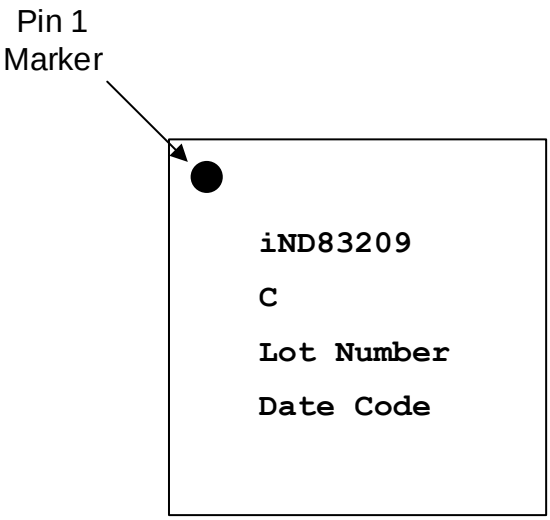
Table 2 QFN20 package dimension

DESCRIPTION		SYMBOL	MILLIMETER		
			MIN	NOM	MAX
TOTAL THICKNESS		A	0.80	0.85	0.90
STAND OFF		A1	0.00	—	0.05
MOLD THICKNESS		A2	0.60	0.65	0.70
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.20	0.25	0.30
BODY SIZE	X	D	3.95	4.00	4.05
	Y	E	3.95	4.00	4.05
LEAD PITCH		e	0.5 BSC		
EP SIZE	X	D1	2.65	2.70	2.75
	Y	E1	2.65	2.70	2.75
LEAD LENGTH		L	0.35	0.40	0.45
LEAD EDGE TO PKG EDGE		Z	0.875 REF		
Tolerance of form and position					
PACKAGE EDGE TOLERANCE	aaa	0.1			
MOLD FLATNESS	bbb	0.1			
COPLANARITY	ccc	0.08			
LEAD OFFSET	ddd	0.1			
EXPOSED PAD OFFSET	eee	0.1			

6.2.2 Part Number

Part Number: iND83209

Package Branding:



6.3 IO PIN DESCRIPTIONS

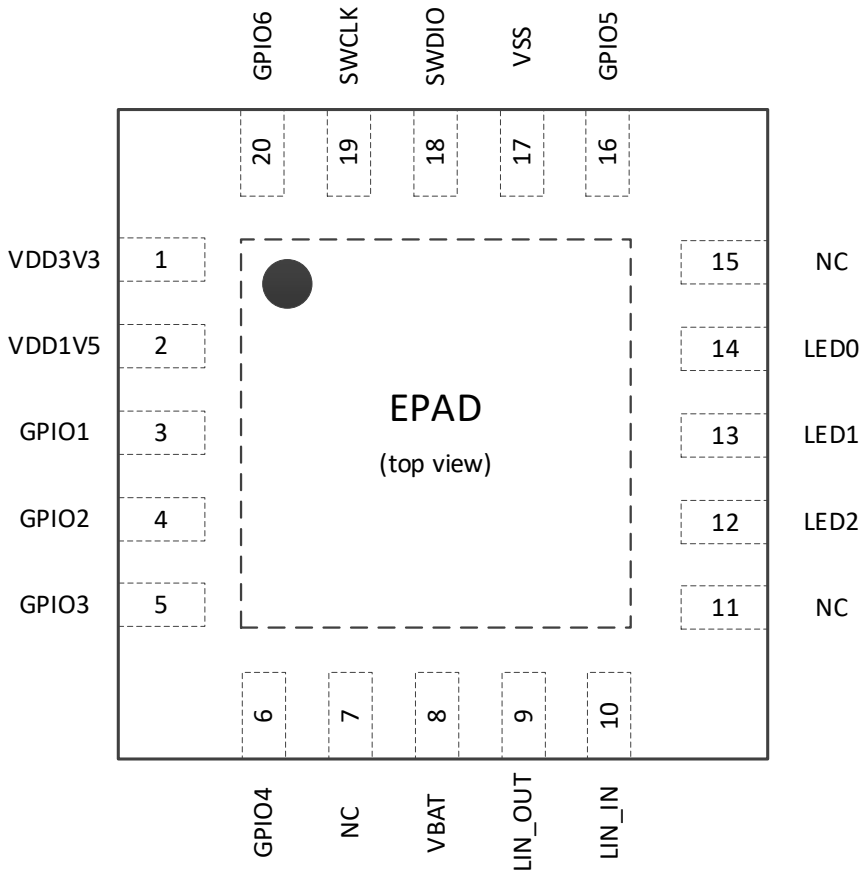


Figure 3 Pin Configuration

Table 3 Pin List

#	Pin Name	Type	Voltage	Direction	Description
1	VDD3V3	Supply	3.3V	n/a	Connect to the external 4.7uF capacitor. Also used for debugger detection.
2	VDD1V5	Supply	1.5V	n/a	Connect to the external 4.7uF capacitor.
3	GPIO1	GPIO	VDD3V3	I/O	General purpose IO/LINM RxD
4	GPIO2	GPIO	VDD3V3	I/O	General purpose IO/LINM TxD
5	GPIO3	GPIO	VDD3V3	I/O	General purpose IO/LINS RxD

#	Pin Name	Type	Voltage	Direction	Description
6	GPIO4	GPIO	VDD3V3	I/O	General purpose IO/LINS TxD
7	NC				
8	VBAT	Supply	Vehicle Power	n/a	
9	LIN_OUT	IO	Pulled up to Vehicle Power	I/O	J2602 LIN 2.x
10	LIN_IN	IO	Pulled up to Vehicle Power	I/O	J2602 LIN 2.x
11	NC				
12	HVIO2/LED2	Output	Vehicle Power	Analog	
13	HVIO1/LED1	Output	Vehicle Power	Analog	High Voltage Open Drain/Collector Current Regulated Sink Firmware controlled current
14	HVIO0/LED0	Output	Vehicle Power	Analog	High Voltage Open Drain/Collector Current Regulated Sink Firmware controlled current
15	NC				
16	GPIO5			I/O	General purpose IO/LINS RxD
17	VSS	Supply	GND	Analog	Bonding with ground plane
18	SWDIO	GPIO	VDD3V3	I/O	ARM debugger data. Integrated weak pull up.
19	SWCLK	GPIO	VDD3V3	Input	ARM debugger clk. Integrated weak pull down.
20	GPIO6				General purpose IO/LINS TxD
*	EPAD	Supply	GND	n/a	Ground

*GND pin is the thermally significant pin

6.3.1 Pin state upon Power-on Reset

- Unless otherwise noted, all pins default to tristate/Isolation mode (Hi-Z) upon power-on reset.

7 ELECTRICAL CHARACTERISTICS

7.1 ABSOLUTE MAXIMUM RATINGS

Table 4 Absolute Maximum Ratings, Voltages Referenced to ground

Names	Conditions	Min.	Max.	Unit
VBAT	No damage, t<500ms	-0.3	+45	V
VBAT	No damage, t<5min	-0.3	+28	V
VBAT	No damage, t<5ms	-1.1		V
VBAT	No damage, t<20ns	-4.0		V
VBAT	No damage, ISO 7637-2 pulse 1, VBAT=13.5V, TA=23°+/-5C, test pulse applied to VBAT via reverse polarity diode and more than 4.7uF capacitor	-100		V
VBAT	No damage, ISO 7637-2 pulse 2 VBAT=13.5V, TA=23°+/-5C, test pulse applied to VBAT via reverse polarity diode and more than 4.7uF capacitor		+50	V
VBAT	No damage, accept ISO 7637-2 pulses 3A, 3B, VBAT=13.5V, TA=(23+/-5)°C, test pulse applied to VBAT via reverse polarity diode and more than 4.7uF capacitor	-150	+100	V
VBAT	No damage, ISO 7637-2 pulses 5b VBAT=13.5V, TA=(23+/-5)°C, test pulse applied to VBAT via reverse polarity diode and more than 4.7uF capacitor		+45	V
LIN	No damage, t<500ms	-40	+40	V
LIN	No damage, ISO 7637-3 pulse 1 VBAT=13.5V, TA=23°+/-5C, test pulse applied to LIN via 1nF capacitor	-100		V
LIN	No damage, ISO 7637-2 pulse 2 VBAT=13.5V, TA=23°+/-5C, test pulse applied via 1nF capacitor		+50	V

LIN	No damage, ISO 7637-2 pulses 3A, 3B VBAT=13.5V, TA= (23+/-5) °C, test pulse applied via 1nF capacitor	-150	+100	V
HVIO	No damage, t<500ms	-0.3	+45	V
HVIO	No damage, t<5min	-0.3	+28	V
HVIO	No damage, t<5ms, voltage applied on the anode side of the LED, current sink open (LED Off)	-1.1		V
HVIO	No damage, t<20ns, voltage applied on the anode side of the LED, current sink open (LED Off)	-4		V
GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, SWDCLK, SWDIO		-0.3	3.6	V
VBAT/LIN_IN/ LIN_OUT to GND	ESD HBM	-4	+4	kV
All pins except VBAT and LIN	ESD HBM	-2	+2	kV
All pins	ESD CDM	-750	+750	V
Storage Temp		-55	+150	°C

Note: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. The absolute maximum ratings provided in the table above are limiting values that do not lead to a permanent damage of the part. But functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ELECTRICAL CHARACTERISTICS

Table 5 Electrical Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit
Operation Conditions					
Operating ambient Temperature		-40	25	125	°C
Operating Junction Temperature		-40	25	125	°C
Package Thermal Resistance	Junction to Ambient (ThetaJA)		30		K/W
VBAT		6	13.5	18	V
IO Supply (VDD3P3)		3.0	3.3	3.6	V
ASIC Core Supply (VDD3P3)		3.0	3.3	3.6	V
MCU Core Supply	MCU Core Supply including SRAM and Flash	1.35	1.5	1.65	V
Flash Memory					
Sector Endurance		20k			cycles
Data Retention	@25degC	100			Years
Data Retention	@85degC	25			Years
SRAM					
Min Retention Voltage	Minimum Retention Voltage below which SRAM data are not guaranteed.	1.08			V
Clocks					
System RC Oscillator Frequency		8		16	MHz
System RC Oscillator Accuracy	16MHz	-5		5	%
System RC Oscillator start up time			10		us

Parameter	Conditions	Min.	Typ.	Max.	Unit
Auxiliary system clock	Used in hibernate mode		16		kHz
Auxiliary system clock Accuracy		-10		10	%
POR/BOR					
POR (VDD3P3)		1.8		2.1	V
BOR VDD3P3	200mV window, steps every 100mV (2.3 to 3.2V)	2.3		3.2	V
BOR VDD1P5	Max Value at which system resume operation			1.6	V
Battery Monitor					
Under Voltage Threshold	Analog Comparator Generates interrupt to MCU except in Hibernate mode (disabled feature)	4.5	5.0	5.5	V
		5.5	6.0	6.5	V
		6.5	7.0	7.5	V
		7.5	8.0	8.5	V
		8.5	9.0	9.5	V
Under Voltage hysteresis	Programmable	0.12	0.2	0.35	V
Under Voltage Digital debounce time	Programmable for signal rise and fall, 62.5ns or 62.5us steps			16	ms
Over Voltage Threshold	Analog Comparator, generates interrupt to MCU except in Hibernate mode (disabled feature)	14		19	V
Over Voltage Hysteresis	Programmable	0.4	1.1	2.4	V
Over Voltage Digital debounce time	Programmable for signal rise and fall, 62.5ns or 62.5us steps			16	ms
Current Source HVIO(LED)					
HVIO voltage	minimum voltage to ensure current regulation			1.6	V
Sink Current	VBAT>6V	0.12		60	mA
Sink Current step size			120		uA

Parameter	Conditions	Min.	Typ.	Max.	Unit
Sink Current Error	Ta=25degC	-7		+7	%
Temperature Drift			-0.025		%/K
HVIO switch resistance	Guaranteed by design	53			Ω
Over Temperature Monitor					
Overtemp Threshold	Analog Comparator, generates interrupt or reset to MCU.	90		165	degC
Overtemp hysteresis		-10			degC
Temperature Sensor					
Temperature range	The MCU is in charge to pull the ADC related data from temperature sensor.	-40		150	degC
Temperature Accuracy		-10		+10	degC
Active current			20		uA
Differential Amplifier for LED VFW measurement					
Input Voltage Range (Vin)	>4V @Gain=1/4	VBAT-4		VBAT	V
	>4V @Gain=1/8	VBAT-8		VBAT	V
Output Voltage Range	Internal output range of LED Sense	0	Vin*Gain	Vref (ADC)	ms
Output Voltage Relative Error				1	%
Gain	Programmable		1/4 or 1/8		
Wake Up					
TWAKEUP	LIN_IN/LIN_OUT, programmable	30	150	200	us
Wake Up Timer	Wakeup Time = 2^(WUT_TAPSEL)/10kHz clock WUT_SEL=0 to 15, default 0	0.1		3276.8	ms
ASIC Watchdog timer					
Timeout	Programmable(See 8.2.6.1)	0.064		8	s

Parameter	Conditions	Min.	Typ.	Max.	Unit
SAR ADC					
Resolution			10		bits
Conversion Speed	17 cycles per conversion (4 cycles for S/H and 13 cycles for conversion)			200	ks/s
ADC Clock	16MHz RC clock divided by 4			4	MHz
INL	Guaranteed by design	-2		2	LSB
DNL	Guaranteed by design	-1		1	LSB
TCURR	Minimum time to wait after the positive edge of the sync input before starting the 1st conversion of the sequence to cover ADC input buffer transient time. Programmable Value (TCURR+1)x250ns, TCURR=7 to 15	2		4	us
TGUARD	Minimum guard time during which there is no channel input selected. (TGUARD+1)x250ns Programmable Value, default 1us	0.25	1	4	ns
TCHNL	Minimum time to wait after TGUARD time to start a new ADC conversion. Programmable Value (TCHNL+1)x250ns, TCHNL=7 to 15	2		4	us
Reference voltage		1.10	1.20	1.30	V
LIN EC specified with VBAT=8V to 16V – refer to LIN 2.x specification, VBUS=LIN pin/line					
Supply Voltage	supply voltage range	6	13.5	18	V
IBUS_LIM	Current Limitation for Driver dominant state driver on VBUS = VBAT=16V	40		200	mA
Rslave	Lin Slave Pullup	20	30	60	kΩ
Rmaster	Lin Master Pullup	900	1000	1100	Ω

Parameter	Conditions	Min.	Typ.	Max.	Unit
IBUS_PAS_dom	Input Leakage Current at the Receiver including Pull-Up Resistor driver off VBUS = 0V VBAT= 12V	-1			mA
IBUS_PAS_rec	Driver off, VBUS>VBAT 8V<VBAT<16V 8V<VBUS<16V			20	uA
IBUS_no_GND	Control unit disconnected from ground GND Device = VSUP 0V<VBUS<16V VBAT = 12V Loss of local ground must not affect communication in the residual network. **LIN 2.2A**	-1		+1	mA
Device Bus Leakage Current Ground Disconnected	VBAT= VGND=12V, 0V<VBUS<18V **J2602**	-100		100	uA
IBUS_no_BAT	VBAT disconnected 0<VBUS<16V, VBAT=0V **LIN 2.2A** Node has to sustain the current that can flow under this condition. Bus must remain operational under this condition.			100	uA
Device Bus Leakage current VBAT disconnected	0V<VBUS<18V, VBAT=VGND=0V **J2602**	-23		23	uA
BUS_VOL Transmitter dominant voltage	Load 500Ohms, driver open drain active	0.0		0.2	VSUP
BUS_VOH Transmitter recessive voltage	Driver open drain high impedance	0.8		1.0	VSUP

Parameter	Conditions	Min.	Typ.	Max.	Unit
CSLAVE	LIN pin input capacitance Note that LIN 2.2A spec 220pF typ, 250pF max as total node capacitance at the connector including the physical bus driver and all other components including C_{LIN}			35	pF
VBUSdom	Receiver dominant state			0.4	VSUP
VBUSrec	Receiver recessive state	0.6			VSUP
VBUS_CNT	Center point Receiver VBUS_CNT =(Vth_dom+ Vth_rec)/2	0.475	0.5	0.525	VSUP
Vhys	Receiver hysteresis VHYS = Vth_rec -Vth_dom			0.175	VSUP
Trx_pd	propagation delay of receiver C_{RXD} load 20pF (RX output of transceiver, internal node, access in test mode) minimum slew rate for the LIN rising and falling edges is 50V/us			6	us
Trx_sym	symmetry of receiver propagation delay rising edge w.r.t. falling edge C_{RXD} load 20pF C_{RXD} load 20pF (RX output of transceiver, internal node, access in test mode)	-2		+2	us
LIN Timing parameters (CBUS ; RBUS): (1nF; 1kΩ) / (6.8nF;660Ω) / (10nF;500Ω)					
D1 Duty Cycle (20kbits/s)	THRec(max) = 0.744 x VSUP; THDom(max) = 0.581 x VSUP; VSUP = 7.0V...16V; tBit = 50µs; D1 = tBus_rec(min) / (2 x tBit)	0.396			-
D2 Duty Cycle (20kbits/s)	THRec(min) = 0.422 x VSUP; THDom(min) = 0.284 x VSUP; VSUP = 7.6V...16V; tBit = 50µs; D2 = tBus_rec(max) / (2 x tBit)			0.581	-

Parameter	Conditions	Min.	Typ.	Max.	Unit
D3 Duty Cycle (10.4kbits/s)	THRec(max) = 0.778 x VSUP; THDom(max) = 0.616 x VSUP; VSUP = 7.0V...16V; tBit = 96µs; D3 = tBus_rec(min) / (2 x tBit)	0.417			-
D4 Duty Cycle (10.4kbits/s)	THRec(min) = 0.389 x VSUP; THDom(min) = 0.251 x VSUP; VSUP = 7.6V...16V; tBit = 96µs; D4 = tBus_rec(max) / (2 x tBit)			0.590	-
tBus_rec(max)-tBus_dom(min)	Δt3, 10.4kbs operation, low speed mode, **J2602**			15.9	us
tBus_dom(max)-tBus_rec(min)	Δt4, 10.4kbs operation, low speed mode, **J2602**			17.28	us
GPIOs					
GPIOVIL	Input Low Voltage			0.3* VDD3P3	V
GPIOVIH	Input High Voltage	0.7* VDDD3P3			V
GPIOIOL	Max load current with output voltage=VOL			10	mA
GPIOIOH	Max load current with output voltage=VOLH			10	mA
GPIOVOL	Output Low Voltage			0.4	V
GPIOVOH	Output High Voltage	2.4			V
GPIOPU	Pull Up Resistance			110	kOhm
GPIOPD	Pull Down Resistance			110	kOhm
SWDCLK, SWDIO					
SWDVIL				0.8	V
SWDVIH		2			V

Parameter	Conditions	Min.	Typ.	Max.	Unit
SWDCLKIOL	SWCLK, Max load current with output voltage=VOL			4	mA
SWDCLKIOH	SWCLK, Max load current with output voltage=VOH			4	mA
SWDIOIOL	SWDIO, Max load current with output voltage=VOL			8	mA
SWDIOIOH	SWDIO, Max load current with output voltage=VOH			8	mA
SWDVOL				0.4	V
SWDVOH		2.4			V
SWDPU (SWDIO IO)	Pull Up Resistance	22		110	kOhm
SWDPD (SWDCLK IO)	Pull Down Resistance	22		110	kOhm
SWDVIL				0.8	V

Electrical Characteristics are valid over the full temperature range of Tj = -40°C to +125°C and a supply range of 6V ≥ VBAT ≤ 18V unless otherwise noted.

The figure below shows the relation between the propagation delay, the TX thresholds and associated receiver duty cycles. Refer to D1 to D4 duty cycles in the table above for THRec and THDom threshold levels.

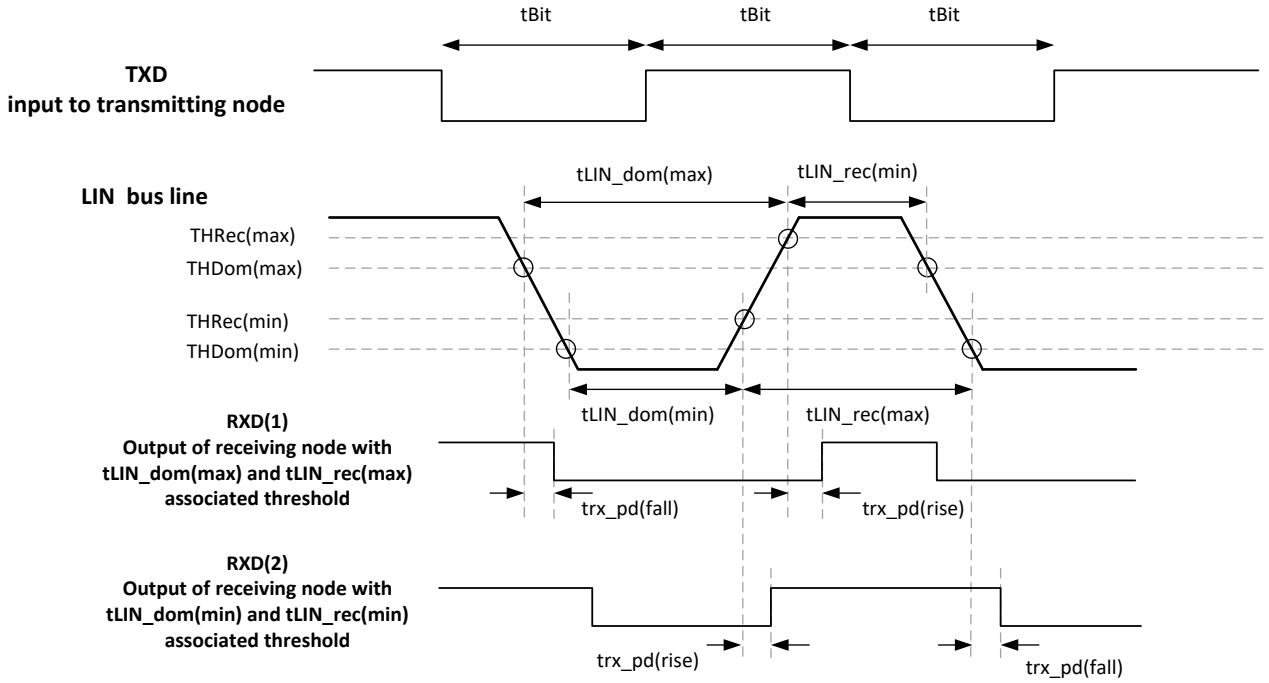


Figure 4 LIN timing Diagram

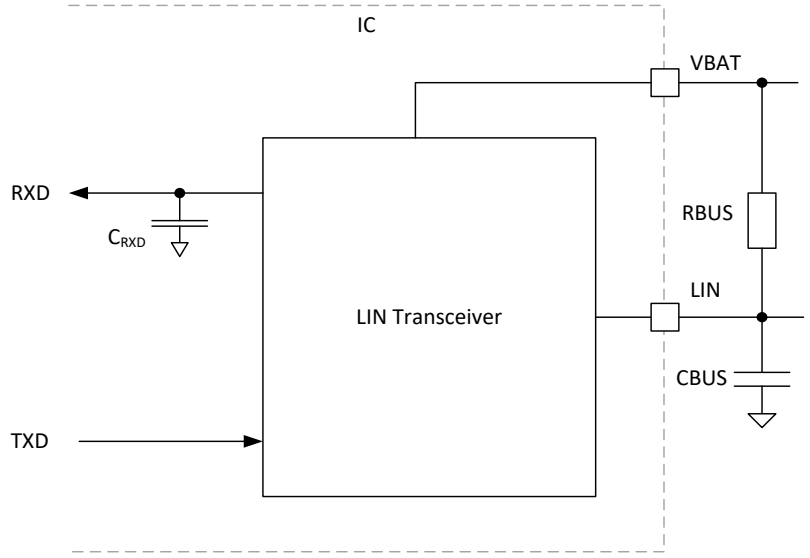


Figure 5 LIN AC Test Circuit

7.3 CURRENT CONSUMPTION

Table 6 Current Consumption					
Mode	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Normal	Ta=85C, VBAT=18V, RCO=16MHz, full functionality: MCU running, no flash write, LED OFF, ADC ON, VBAT and TEMP monitor ON, WDT ON.			10	mA
Hibernate Mode1	Main regulator (3.3V) ON, Load dump protection active. Ta=85degC max, VBAT=13.5V Overvoltage/Undervoltage detection, PWM, LED driver, Tempsensor and ADC are OFF except LIN Switch on and GPIO toggling and wake up timer.	70	85	100	uA
Hibernate Mode2	Main regulator (3.3V) ON, Load dump protection active. Ta=85degC max, VBAT=13.5V Overvoltage/Undervoltage detection, PWM, LED driver, Tempsensor and ADC are OFF except one LIN RX on and GPIO toggling and wake up timer.	60	75	90	uA

7.4 POWER ON AND OFF SLOPE

Table 7 The Slowest rising and falling of the supply voltage

Parameter	Conditions	Min	Max	Unit
VBAT rising rate	Refer to VW80000 test conditions[1]	0.5		V/min
VBAT falling rate	Refer to VW80000 test conditions[1]	0.5		V/min

Note1:See Appendix A.

8 MEMORY DESCRIPTION

8.1 TOP LEVEL MEMORY MAP

The chip uses a unified memory model with a linear address space (Von Neumann architecture) including Flash and RAM memories as well as registers address space. The implementation of the Cortex M0 core uses a high density 64KB Flash cell along with 16KB of SRAM.

Table 8 Top Level Memory Map

Address	Memory	Description
0x00000000 – 0x0000FFFF	Flash	64Kbytes of Flash Memory, user programmable.
0x00010000 – 0x0003FFFF	N/A	Reserved
0x00040000 – 0x000400FF	N/A	Reserved
0x00040100 – 0x000401FF	N/A	Reserved
0x00040200 – 0x1FFFFFFF	N/A	Reserved
0x20000000 – 0x20003FFF	SRAM	16Kbytes of SRAM
0x20004000 – 0x4FFFFFFF	N/A	Reserved
0x50000000 - 0x5000003F	CRGA	Clock & Reset Generator
0x50000040 - 0x5000005F	PMU	Power Management Unit
0x50000060 - 0x5000007F	EVTHOLD	Event Hold Control

0x50010100 - 0x500101FF	WICA	WakeUp Interrupt Controller
0x50010300 - 0x500103FF	WDTA	Watchdog Timer Registers
0x50010600 - 0x500106FF	PWM	Control (and status) registers for the pulse width modulation waveform generator.
0x50010700 - 0x500107FF	LINS	LIN slave interface registers
0x50010800 - 0x50010BFF	LINM	LIN master interface registers
0x50010D00 - 0x50010DFF	ADC	ADC Control
0x50011000 - 0x50011FFF	IOCTRLA	I/O configuration and DFT pin control
0x50012000 - 0x50013FFF	SYSCTRLA	System configuration and retention memory
0x50018000 - 0x5001FFFF	GPIO	GPIO bit control and configuration
0x50000080 - 0x500000FF	BTE	Block Transfer Engine registers
0x50020000 - 0x50020007	TIMER0	General purpose timer 0
0x50020008 - 0x5002000F	TIMER1	General purpose timer 1
0x50020010 - 0x50020017	TIMER2	General purpose timer 2
0x50020018 - 0x5002001F	WDT1	The watchdog timer that is local to the MCU

0x50020020 – 0x5002005F	Flash	Flash Programming/Erase Control
0x50020048 – 0xDFFFFFFF	N/A	Reserved
0xE0000000 – 0xE00FFFFF	Private peripheral bus	ARM peripherals
0xE0100000 – 0xEFFFFFFF	N/A	Reserved
0xF0000000 – 0xF0001FFF	System ROM tables	ARM core IDs
0xF0002000 – 0xFFFFFFFF	N/A	Reserved

8.2 Register Descriptions

8.2.1 Clock & Reset Generator

CRGA		
Address	**Register Name**	**Description**
0x50000000	LFCLKCTRL	Low frequency clock control
0x50000004	SYSCLKCTRL	System clock control
0x50000008	RESETCTRL	Reset control
0x5000000C	MODULERST	Module Reset control
0x50000010	BORACTION	BOR action
0x50000014	BORCONFIG	BOR configuration
0x50000018	WDTACTION	Watchdog action
0x5000001C	LFCLKKILL	Low frequency clock kill
0x50000020	CPCLKCTRL	Charge pump clock control
0x50000024	OVTEMPACTION	OVTEMP action
0x50000028	OVTEMPCONFIG	OVTEMP configuration

8.2.1.1 LFCLKCTRL

0x50000000	LFCLKCTRL	^

Low frequency clock control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F8	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F8	CLKLFSEL	LF Clock Source select. Used to select lf osc mode between 0x0: CLK_LF(LF OSC out) is 32KHz, slow system clock freq is Freq_CLK_LF/2. 0x1: CLK_LF(LF OSC out) is 256KHz, slow system clock freq is Freq_CLK_LF/16. Recommended for more accurate LIN Wakeup detection in hibernate mode.	1	rw	0x0
F0	LFRCSTS	Slow oscillator status. Will be high when the 16KHz oscillator is selected	1	ro	0x0

8.2.1.2 SYSCLKCTRL

0x50000004 **SYSCLKCTRL** ^

System clock control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	F16			-	-	-	-	-	-	-	F8	-	-	-	-	-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F16	DIVSYSCLK	Clock div select. Select the divider ratio on the system clock when using fast oscillator 0x0: No Division. Full Clock speed. 0x1: Div by 2. 0x2: Div by 3. 0x3: Div by 4. 0x4: Div by 5. 0x5: Div by 6. 0x6: Div by 7. 0x7: Div by 8.	3	rw	0x0

F8	SYSCLKSEL	Clock select. Used to switch between the fast and slow system clocks 0x0: Slow clock (16 KHz) 0x1: Fast clock (16 MHz)	1	rw	0x0
F1	HFRCSTS	Fast oscillator status. Will be high when the 16MHz oscillator is enabled	1	ro	0x0
F0	HFRCENA	Fast oscillator enable. Setting this bit when the 16MHz oscillator is not running will cause the oscillator to start (the PMU may have already started it). Even though the fast oscillator is running, its output is only used when selected via the clock mux - see CLKSEL. This bit is cleared automatically on entering SLEEP mode	1	rw	0x0

8.2.1.3 RESETCTRL

0x50000008 RESETCTRL ^

Reset control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F24	-	-	-	-	-	-	-	F16	-	F14	F13	F12	-	F10	-	F8	-	F6	F5	F4	-	F2	-	F0

#	Field Name	Field Description	Width	Access	Reset
F24	SOFTRSTREQ	Soft reset request. Set to trigger a soft reset of chip Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F16	HARDRSTREQ	Hard reset request. Set to trigger a hard reset of chip	1	wo	0x0
F14	OVTEMPFLAGCLR	OVTEMP flag clear. Set to clear the OVTEMP flag	1	wo	0x0
F13	WDTFLAGCLR	WDT flag clear. Set to clear the WDT flag	1	wo	0x0
F12	BOR1V5FLAGCLR	BOR 1v5 clear. Set to clear the 1.5V brownout detected flag	1	wo	0x0

F10	BOR3V3FLAGCLR	BOR 3v3 clear. Set to clear the 3.3V brownout detected flag	1	wo	0x0
F8	PORFLAGCLR	POR flag clear. Set to clear the POR flag	1	wo	0x0
F6	OVTEMPFLAG	Over Temp Violation flag. Set by the hardware when the over temp condition is detected.	1	ro	N/A
F5	WDTFLAG	Watchdog bark flag. Set by the hardware when the watchdog barks.	1	ro	N/A
F4	BOR1V5FLAG	BOR 1v5 flag. Set by the hardware when a brownout of the 1.5V supply is detected.	1	ro	0x0
F2	BOR3V3FLAG	BOR 3v3 flag. Set by the hardware when a brownout of the 3.3V supply is detected.	1	ro	0x0
F0	PORFLAG	Power on reset flag. Set by the hardware during power-on reset	1	ro	N/A

8.2.1.4 MODULERST

0x5000000C **MODULERST** ^

Module Reset control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0			

#	Field Name	Field Description	Width	Access	Reset
F0	MODULERSTREQ	Module Soft reset request. Set to trigger a soft reset of module below. 0x1: ADC Soft reset request 0x2: LINM Soft reset request 0x4: LINS Soft reset request 0x8: PWM soft reset request Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	4	wo	0x0

8.2.1.5 BORACTION

0x50000010	BORACTION	^

BOR action.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	-	-	-	-	F23	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F4		-	-	F0	

#	Field Name	Field Description	Width	Access	Reset
F31	BOR_1V5_LOCK	Set Only bit. Set this bit to lock BOR_1V5_ACTION & BOR_1V5_THRESH bits.	1	rw	0x0
F23	BOR_3V3_LOCK	Set Only bit. Set this bit to lock BOR_3V3_ACTION & BOR_3V3_THRESH bits.	1	rw	0x0
F4	VDD1V5	BOR 1v5 action. Defines the consequences of brown-out condition on the 1v5 supply being detected by the hardware. 0x2: No action 0x1: IRQ generated 0x0: Hard reset generated	2	rw	0x0
F0	VDD3V3	BOR 3v3 action. Defines the consequences of brown-out condition on the 3v3 supply being detected by the hardware. 0x2: No action 0x1: IRQ generated 0x0: Hard reset generated	2	rw	0x0

8.2.1.6 BORCONFIG

0x50000014	BORCONFIG	^

BOR configuration.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	F28	-	-	-	F24	-	-	-	-	F16				-	-	-	-	-	-	-	-	-	-	-	-	F0			

#	Field Name	Field Description	Width	Access	Reset
F28	BORBIASOVERRIDESEL	BOR bias override select. Independently controllable test bit which can be used to override the BOR bias enable signal. Set 1 to enable the use of the BOR_REF_ENA register test bit. 0x0: Functional Mode 0x1: Override Mode- Use BOR_BIAS_OVERRIDE_ENA register to control bias.	1	rw	0x0
F24	BORBIASOVERRIDEENA	BOR bias override bit. Independently controllable test bit which can be used to override the BOR bias enable signal. Set 1 to enable the use of this test bit.	1	rw	0x1
F16	BOR1V5THRESH	BOR 1v5 threshold. Select the BOR threshold voltage level for the 1v5 regulator. Following typical value(under 27degC) can be used as reference: 0x0: Vr: 1.317V Vf: 1.261V 0x1: Vr: 1.347V Vf: 1.290V 0x2: Vr: 1.379V Vf: 1.320V 0x3: Vr: 1.412V Vf: 1.352V 0x4: Vr: 1.446V Vf: 1.385V 0x5: Vr: 1.482V Vf: 1.420V 0x6: Vr: 1.520V Vf: 1.456V 0x7: Vr: 1.560V Vf: 1.495V 0x8: Vr: 1.602V Vf: 1.535V 0x9: Vr: 1.646V Vf: 1.578V 0xa: Vr: 1.693V Vf: 1.624V 0xb: Vr: 1.743V Vf: 1.672V 0xc: Vr: 1.796V Vf: 1.723V 0xd: Vr: 1.852V Vf: 1.777V 0xe: Vr: 1.911V Vf: 1.835V 0xf: Vr: 1.975V Vf: 1.896V	4	rw	0x3
F0	BOR3V3THRESH	BOR 3v3 threshold. Select the BOR threshold voltage level for the 3v3 regulator, Following typical value(under 27degC) can be used as reference: 0x0: Vr: 2.193V Vf: 2.101V 0x1: Vr: 2.256V Vf: 2.161V 0x2: Vr: 2.322V Vf: 2.225V 0x3: Vr: 2.392V Vf: 2.293V 0x4: Vr: 2.466V Vf: 2.365V 0x5: Vr: 2.546V Vf: 2.442V 0x6: Vr: 2.631V Vf: 2.524V	4	rw	0x6

		0x7: Vr: 2.721V Vf: 2.612V 0x8: Vr: 2.819V Vf: 2.706V 0x9: Vr: 2.924V Vf: 2.807V 0xa: Vr: 3.037V Vf: 2.916V 0xb: Vr: 3.159V Vf: 3.034V 0xc: Vr: 3.291V Vf: 3.162V 0xd: Vr: 3.435V Vf: 3.300V 0xe: Vr: 3.593V Vf: 3.451V 0xf: Vr: 3.765V Vf: 3.617V			

8.2.1.7 WDTACTION

0x50000018	WDTACTION	^

Watchdog action.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F16	-	-	-	-	F8				-	-	-	F1				F0

#	Field Name	Field Description	Width	Access	Reset
F16	WDTBARKCNTCLR	WatchDog Bark Counter Clear. Set to clear watchdog bark counter.	1	wo	0x0
F8	WDTBARKCNT	WatchDog Bark Counter. Read to reflect the WDT bark counter value.	4	ro	0x0
F0	WDTACTION	Watchdog action. Defines the consequences of watchdog bark being detected by the hardware. 0x0: IRQ generated 0x1: Hard reset generated	1	rw	0x1

8.2.1.8 LFCLKKILL

0x5000001C	LFCLKKILL	^

Low frequency clock kill.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	KILLLFRC	Kill slow RC oscillator. Setting this bit gates the low frequency RC oscillator input	1	rw	0x0

8.2.1.9 CPCLKCTRL

0x50000020 CPCLKCTRL ^

Charge pump clock control. The clock divider and the charge pump clock gate use the system clock as the clock source. The charge pump clock divider is fed by the gated clock.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F4		-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F4	PMUCPDIVSEL	PMU charge pump divider select. Selects the divide value for the PMU Charge Pump Clock. 0x0: No Division. Full Clock speed. 0x1: Div by 2. 0x2: Div by 4. 0x3: Div by 8. 0x4: Div by 16. 0x5: Div by 32.	3	rw	0x2
F1	PMUCPREG	PMU charge pump override register. If the PMU_CP_SEL bit is high, setting this bit will enable the PMU charge pump clock gate.	1	rw	0x0
F0	PMUCPSEL	PMU charge pump select. Setting this bit will override the enable signal to the PMU charge pump clock gate. 0x0: The PMU charge pump clock gate is enabled by two sources by default: 1. The PMU state machine 'bring-up/active' states (i.e. hardware driven) 2. The High Frequency Oscillator being active *Note* both #1	1	rw	0x0

		and #2 soures must be active. 0x1: The value of the PMU_CP_REG field is what is used to drive the enable signal on the PMU charge pump clock gate. *Note* this allows the charge pump clock to be driven even with the slow RC oscillator (16KHz).			

8.2.1.10 OVTEMPACTION

0x50000024	OVTEMPACTION	^

OVTEMP action.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0	

#	Field Name	Field Description	Width	Access	Reset
F31	OVTEMP_LOCK	Set Only bit. Set this bit to lock OVTEMP related bits.	1	rw	0x0
F0	OVTEMP	Over Temperature action. Defines the consequences of over temp condition detected by the hardware. 0x2: No action 0x1: IRQ generated 0x0: Hard reset generated	2	rw	0x0

8.2.1.11 OVTEMPCONFIG

0x50000028	OVTEMPCONFIG	^

OVTEMP configuration.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	F25	F24	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0			

#	Field Name	Field Description	Width	Access	Reset
F25	DISTEMPSENS	Disable Temp Sensor Analog Part. Set to disable Temperature Sensor analog circuit only if OVTEMP_ENA is clearred. Notice that the internal temperature sensor is shared by over temp monitor. BGAUXREG in SYSCTRLA should be enabled before using TempSensor in hibernate mode.	1	rw	0x0
F24	OVTEMPENA	OverTemp Monitor Enable bit.	1	rw	0x0
F0	OVTEMPLEVEL	Over Temp threshold. Select the OVTEMP threshold level for the monitor. 0x0: 90C 0x1: 95C 0x2: 100C 0x3: 105C 0x4: 110C 0x5: 115C 0x6: 120C 0x7: 125C 0x8: 130C 0x9: 135C 0xa: 140C 0xb: 145C 0xc: 150C 0xd: 155C 0xe: 160C 0xf: 165C	4	rw	0xB

8.2.2 Power Management Unit

PMUA		
Address	**Register Name**	**Description**
0x50000040	CTRL	Control

0x50000044	DEBUG	Debug
0x50000048	DWELL	Dwell
0x5000004C	VBATCTRL	VBAT Monitor Register
0x50000050	VBATTRIM	VBAT Monitor Trim Register
0x50000054	VBATDBNC	VBAT Debounce Register
0x50000058	VBATDBNCTHRES	VBAT Monitor Threshold Register
0x5000005C	PMUIRQ	Voltage Monitor interrupts

8.2.2.1 CTRL

0x50000040 CTRL ^

Control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F3	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F3	FASTMCUON	Fast MCU Power On. Set to enable VDD1V5 LDO during hibernate mode for fast mcu power on sequennce. Clr to disable VDD1V5 LDO during hibernate mode for saving power.	1	rw	0x1
F1	FASTBOOT	Fast boot. Set to enable used of the fast clock during subsequent power-up sequences (including the portion consumed by the mcu boot sequence). The set value brings the system up with the slow clock to make the initial boot and any boot after a hard reset (e.g. after a brownout) as safe as possible.	1	rw	0x1
F0	HIBERNATE	Hibernate. Set to put the chip into HIBERATE mode. Before setting this bit, ensure that wake interrupt	1	wo	0x0

		controller HOLD bit has been set (and that a corresponding Lullaby interrupt has been received).			

8.2.2.2 DEBUG

0x50000044 DEBUG ^

Debug.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	IGNORE_CIFS	Ignore QACKs. Setting a bit in this register prevents PMUA from waiting for the assertion of the corresponding 'Quiescent State Acknowlege' signal when before transitioning towards the Hibernate state	1	rw	0x0

8.2.2.3 DWELL

0x50000048 DWELL ^

Dwell. Minimum times spent in various PMUA states. Please Note- The STARTUP_BIAS_DWELL state timeout is hardcoded to a value of 0xC. A value of 0xC in the STARTUP_BIAS_DWELL state @ 16KHz yields a delay of 1.5 milliseconds

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	F20				F16				F12				F8				F4				F0			

#	Field Name	Field Description	Width	Access	Reset
F20	ENABLE_MAIN_REG	Enable main regulator dwell time. Defines the amount of time spent in the 'Enable main reg' state. Allows the main 3v3 regulator to power up before the first load (the bias) is enabled	4	rw	0xC

F16	POWER_DOWN_MCU	Power down MCU dwell time. Defines the amount of time spent in the 'Power down MCU' state. Pausing here allows the MCU supplies to discharge (to guarantee subsequent POR)	4	rw	0xC
F12	ATTACH_3V3	Attach 3.3V dwell time. Defines the amount of time spent in the 'Attach 3V3' state. State Attaches 3.3V to MCU.	4	rw	0xC
F8	ATTACH_1V5	Attach 1.5V dwell time. Defines the amount of time spent in the 'Attach 1V5' state. State Attaches 1.5V to MCU.	4	rw	0xC
F4	ENABLE_1V5	Enable 1.5V dwell time. Defines the amount of time spent in the 'Enable 1V5' state. Allows 3v3 and 1v5 regs to settle	4	rw	0xC
F0	ENABLE_BIAS	Enable bias dwell time. Defines the amount of time spent in the 'Enable bias' state. Allows the 3v3 reg to settle	4	rw	0xC

8.2.2.4 VBATCTRL

0x5000004C	VBATCTRL	^

VBAT Monitor Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	F25	F24	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F25	HIGH	Battery Voltage High Status. RAW battery monitor over voltage event signal coming from the analog comparator circuit.	1	ro	0x0
F24	LOW	Battery Voltage Low Status. RAW battery monitor under voltage event signal coming from the analog comparator circuit.	1	ro	0x0

F3	OV_POL	Battery Voltage Monitor Over Voltage Interrupt Event Polarity. Flips the over voltage event signal coming from the analog comparator circuit which feeds into the interrupt generator. 0x0: Native Polarity 0x1: Flip Polarity	1	rw	0x0
F2	UV_POL	Battery Voltage Monitor Under Voltage Interrupt Event Polarity. Flips the under voltage event signal coming from the analog comparator circuit which feeds into the interrupt generator. 0x0: Native Polarity 0x1: Flip Polarity	1	rw	0x0
F1	OV_MONITOR_ENA	Battery Over Voltage Monitor Enable. Set to enable the vbat over voltage monitor analog comparator circuit.	1	rw	0x0
F0	LOW_MONITOR_ENA	Battery Under Voltage Monitor Enable. Set to enable the vbat under voltage monitor analog comparator circuit.	1	rw	0x0

8.2.2.5 VBATTRIM

0x50000050	VBATTRIM	^

VBAT Monitor Trim Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	F24		-	-	-	-	F16				-	-	-	-	-	-	F8		-	-	F0					

#	Field Name	Field Description	Width	Access	Reset
F24	OVHYS	Battery Voltage Monitor Over Voltage Hysteresis Select. Selects the hysteresis level for the Over Voltage monitor. 0x0: 0.44V 0x1: 1.13V 0x2: 1.77V 0x3: 2.36V	2	rw	0x1
F16	OVLEVEL	Battery Voltage Monitor Over Voltage Select. Selects the reference level for the Over Voltage monitor. If	4	rw	0x7

		OVLEVEL>9, the real analog trim value is the same as OVLEVEL==0. 0x0: Over Voltage Threshold- Vr: 14.72V Vf: 13.97V 0x1: Over Voltage Threshold- Vr: 15.21V Vf: 14.42V 0x2: Over Voltage Threshold- Vr: 15.74V Vf: 14.90V 0x3: Over Voltage Threshold- Vr: 16.30V Vf: 15.41V 0x4: Over Voltage Threshold- Vr: 16.90V Vf: 15.96V 0x5: Over Voltage Threshold- Vr: 17.55V Vf: 16.55V 0x6: Over Voltage Threshold- Vr: 18.24V Vf: 17.18V 0x7: Over Voltage Threshold- Vr: 19.00V Vf: 17.87V 0x8: Over Voltage Threshold- Vr: 19.82V Vf: 18.61V 0x9: Over Voltage Threshold- Vr: 20.72V Vf: 19.42V			
F8	UVHYS	Battery Voltage Monitor Under Voltage Hysteresis Select. Selects the hysteresis level for the Under-Voltage monitor. 0x0: 127mV 0x1: 199mV 0x2: 273mV 0x3: 351mV	2	rw	0x1
F0	UVLEVEL	Battery Voltage Monitor Under Voltage Select. Selects the reference level for the Under Voltage monitor. If UVLEVEL>39, the real analog trim value is the same as UVLEVEL==0. The UVLEVEL threshold is monotonically increasing with the setting. The UVLEVEL setting: 0x0: UV Threshold - Vr: 4.82V Vf: 4.66V 0x9: UV Threshold - Vr: 5.55V Vf: 5.36V	6	rw	0x9

8.2.2.6 VBATDBNC

0x50000054 **VBATDBNC** ^

VBAT Debounce Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F5	OVSTRB1SEL	Low frequency strobing select for debouncing. Enables strobing 1 with the Low frequency clock(16K) instead of just clocking with High frequency Clock(16M).	1	rw	0x0

		Default is set to 0 for quick acknowledgement of OV event.			
F4	OVSTRB0SEL	Low frequency strobing select for debouncing. Enables strobing 0 with the Low frequency clock(16K) instead of just clocking with High frequency Clock(16M). Default is set to 1 for debouncing of OV.	1	rw	0x1
F3	UVSTRB1SEL	Low frequency strobing select for debouncing. Enables strobing 1 with the Low frequency clock(16K) instead of just clocking with High frequency Clock(16M). Default is set to 0 for quick acknowledgement of UV event.	1	rw	0x0
F2	UVSTRB0SEL	Low frequency strobing select for debouncing. Enables strobing 0 with the Low frequency clock(16K) instead of just clocking with High frequency Clock(16M). Default is set to 1 for debouncing of UV.	1	rw	0x1
F1	OV	over voltage signal debounce enable. if set to '1, debounces the over voltage signal before going to over voltage interrupt generation else the signal bypass the debouncer	1	rw	0x1
F0	UV	under voltage signal debounce enable. if set to '1, debounces the under voltage signal before going to under voltage interrupt generation else the signal bypass the debouncer	1	rw	0x1

8.2.2.7 VBATDBNCTHRES

0x50000058 **VBATDBNCTHRES** ^

VBAT Monitor Threshold Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F24								F16								F8								F0							

#	Field Name	Field Description	Width	Access	Reset
F24	OVTHRES0	Over Voltage debouncing threshold for 1to0 Transition. Sets the threshold for debouncing the over voltage	8	rw	0xFF

		event going from 1 to 0. It will require the ov event to stay high for the (OVTHRES0+1) number of LF/HF clocks to transit from a 1 to 0.			
F16	UVTHRES0	Under Voltage debouncing threshold for 1to0 Transition. Sets the threshold for debouncing the under-voltage event going from 1 to 0. It will require the uv event to stay high for the (UVTHRES0+1) number of LF/HF clocks to transit from a 1 to 0.	8	rw	0xFF
F8	OVTHRES1	Over Voltage debouncing threshold for 0to1 Transition. Sets the threshold for debouncing the over voltage event going from 0 to 1. It will require the ov event to stay high for the (OVTHRES1+1) number of LF/HF clocks to transit from a 0 to 1.	8	rw	0x1
F0	UVTHRES1	Under Voltage debouncing threshold for 0to1 Transition. Sets the threshold for debouncing the under-voltage event going from 0 to 1. It will require the uv event to stay high for the (UVTHRES1+1) number of LF/HF clocks to transit from a 0 to 1.	8	rw	0x1

8.2.2.8 PMUIRQ

0x5000005C	PMUIRQ	^

Voltage Monitor interrupts. Contains the the enable, clear, status and active flag for the Battery Voltage interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	F25	F24	-	-	-	-	-	-	F17	F16	-	-	-	-	-	-	F9	F8	-	-	-	-	-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F25	OV	over voltage interrupt active.	1	ro	0x0
F24	UV	under voltage interrupt active.	1	ro	0x0
F17	OV	over voltage interrupt status.	1	ro	0x0
F16	UV	under voltage interrupt status.	1	ro	0x0

F9	OV	over voltage interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F8	UV	under voltage interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F1	OV	over voltage interrupt enable.	1	rw	0x0
F0	UV	under voltage interrupt enable.	1	rw	0x0

8.2.3 Event Hold Control

EVTHOLD		
Address	**Register Name**	**Description**
0x50000060	HOLD	Hold

8.2.3.1 HOLD

0x50000060	HOLD	^

Hold.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	HOLD	Hold. Set to prevent serialization of new non-wakeup events in preparation for hibernate mode. At the point of becoming set, a request to send the lullaby interrupt	1	wo	0x0

		is automatically generated. The lullaby handler can then safely assert the PMUA->CTRL.HIBERNATE bit in order to put the device into hibernate mode.			

8.2.4 Block Transfer Engine

BTE		
Address	**Register Name**	**Description**
0x50000080	BTE_CTRL	BTE Control Register
0x50000084	BTE_SRAM_ADDR	BTE SRAM Address Register

8.2.4.1 BTE_CTRL

0x50000080	BTE_CTRL	^

BTE Control Register. This register can only be written if there is no ongoing transfer. If the BTE is transferring data, any writes to this register will be ignore

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	F27	F26	F25	F24	F16								F0															

#	Field Name	Field Description	Width	Access	Reset
F27	START	An operation is initiated when this bit is set. The bit auto-clears when the block is complete.	1	rw	0x0
F26	BLOCKING	If set then the block transfer has priority over the MCU. If the MCU tries to use the bus, it will stall until the block transfer is complete. If not set, then the MCU waits only until the remainder of the current word completes and then waits until the bus is idle again before continuing.	1	rw	0x0
F25	TX_DIR	Transfer direction. If set then SRAM->ASIC otherwise ASIC->SRAM	1	rw	0x0

F24	INC_ADDR	if set then ASIC die address increments at the end of each transfer. Set to zero if the peripheral is a FIFO.	1	rw	0x0
F16	BXNUM	Number of 32-bit words to transfer.	8	rw	0x0
F0	BXADD	Address of the ASIC die (LSB). This is the lower 16 bits of the ASIC die address. The MSBs are 0x5001.	16	rw	0x0

8.2.4.2 BTE_SRAM_ADDR

0x50000084	BTE_SRAM_ADDR	^

BTE SRAM Address Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	BXSRAMADDR	Address of the SRAM (LSB). This is the lower 16 bits of the SRAM address. The MSBs are 0x2000.	16	rw	0x0

8.2.5 WakeUp Interrupt Controller

WICA		
Address	**Register Name**	**Description**
0x50010100	CTRL	Wakeup Control Register
0x50010104	STATUS	Wakeup Status Register

8.2.5.1 CTRL

0x50010100	CTRL	^

Wakeup Control Register. This is the control register for wakeup via lin or wut

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F15	F14	-	F12	F11	F10	-	F8	F4				F3	F2	-	F0

#	Field Name	Field Description	Width	Access	Reset
F15	LINMIRQCLR	clear the wulin_irq. writting a '1 to this register will clear the wulins_irq	1	wo	0x0
F14	TIMERIRQCLR	clear the wutimer_irq. writting a '1 to this register will clear the wutimer_irq	1	wo	0x0
F12	LINSIRQCLR	clear the wulin_irq. writting a '1 to this register will clear the wulins_irq	1	wo	0x0
F11	LINMIRQENA	LIN Master Wakeup Interrupt Enable. if set, wulinm_irq is asserted if a wakeup signal is detected on the LIN_OUT bus	1	rw	0x0
F10	TIMERIRQENA	Timer Wakeup Interrupt Enable. if set, wutimer_irq is asserted if wakeup timer matches the tapsel	1	rw	0x1
F8	LINSIRQENA	LIN Slave Wakeup Interrupt Enable. if set, wulin_irq is asserted if a wakeup signal is detected on the LIN_IN bus	1	rw	0x1
F4	TIMERTAPSEL	WakeUp Timer Tap Select. Wakeup Time = 2^(WUT_TAPSEL) x Tlfclk(62.5us)	4	rw	0x4
F3	LINMENA	LIN Master Wakeup Enable. it enables the detect of a wakeup signal on the LIN_OUT bus	1	rw	0x0
F2	TIMERENA	Wakeup Timer Enable. it enables the wakeup timer	1	rw	0x0

F0	LINSENA	LIN Slave Wakeup Enable. it enables the detect of a wakeup signal on the LIN_IN bus	1	rw	0x0

8.2.5.2 STATUS

0x50010104	STATUS	^

Wakeup Status Register. This is the status register for wakeup via gpio or lin or wut

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																-	-	-	-	-	-	-	-	-	-	-	-	F3	F2	-	F0

#	Field Name	Field Description	Width	Access	Reset
F16	TIMERCNT	Wakeup Timer Counter Value. Counter Value of the Wakeup Timer	16	ro	0x0
F3	LINM	LIN Master Wakeup Status. This gets set if a wakeup signal is detected on the LIN_OUT bus when LINM SLEEP bit is set. CLRIRQ clears this Register	1	ro	0x0
F2	TIMER	Wakeup Timer Status. This gets set if a wakeup timer is enabled and the count matches the tapsel setting during hibernate, CLRIRQ clears this Register	1	ro	0x0
F0	LINS	LIN Slave Wakeup Status. This gets set if a wakeup signal is detected on the LIN_IN bus when LINS SLEEP bit is set. CLRIRQ clears this Register	1	ro	0x0

8.2.6 Watchdog Timer

WDTA		
Address	**Register Name**	**Description**
0x50010300	CTRL	Control
0x50010304	STOP	Stop
0x50010308	CLEAR	Clear
0x5001030C	CNTVAL	Counter value
0x50010310	INT	WDTA Interrupts

8.2.6.1 CTRL

0x50010300 **CTRL** ^

Control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F14	F12		F11		F8		-	-	-	-	-	-	F1	-

#	Field Name	Field Description	Width	Access	Reset
F14	WINOPENFLAG	Window open flag. A flag that indicates when the watchdog window is open. It only can be cleared by Reg CLEAR! 0x0: Window is Closed 0x1: Window is Open	1	ro	0x0
F12	WINOPENSEL	Window Mode open select. Defines the watchdog window open time (the time between the watchdog start and the window open).	2	rw	0x0

		0x0: 1/2 * WDT timeout 0x1: 1/4 * WDT timeout 0x2: 1/8 * WDT timeout 0x3: 1/16* WDT timeout			
F11	WINOPENENA	Window Mode Enable. Enables Window Mode. 1'b1: Enable the Window mode of Watchdog, if the WDT is cleared before the time window opens, the WDT will issue a system reset. 1'b0: Disable the Window mode of Watchdog.	1	rw	0x0
F8	TIMEOUTSEL	Timeout select. Defines the watchdog timeout period (the time between a clear operation and the next timeout). 0x0: 2^11 * 62.5us ~= 128 ms 0x1: 2^12 * 62.5us ~= 256 ms 0x2: 2^13 * 62.5us ~= 512 ms 0x3: 2^14 * 62.5us ~= 1.0 ms 0x4: 2^15 * 62.5us ~= 2.0 s 0x5: 2^16 * 62.5us ~= 4.0 s 0x6: 2^17 * 62.5us ~= 8.0 s 0x7: 2^18 * 62.5us ~= 16.0 s	3	rw	0x7
F1	RUNNING	Running status. A flag that indicates when the watchdog timer is enabled. 0x0: Watchdog timer is stopped and cleared 0x1: Watchdog timer is running	1	ro	0x0
F0	UPDATE	*Window Mode Enable* Set to update Analog-Watchdog Configurations. NOTE: DO NOT change the CTRL register when it is high, which indicates there is an update in progress, It gets cleared by the core when the current update is done	1	dual	0x0

8.2.6.2 STOP

0x50010304	STOP	^

Stop.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F31	STOP_LOCK	Set Only bit. Set this bit to lock STOP bits.	1	rw	0x0
F0	STOP	Stop. Write the *stop* code (0xc3) to this register to reset the timer and disable the watchdog (e.g. during debug). If any other value is written to this register the watchdog will be enabled.	8	rw	0x55

8.2.6.3 CLEAR

0x50010308 CLEAR ^

Clear.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	CLEAR	Clear. Write the value 0x3c574ad6 (as a single word access) to reset the watchdog timer. Periodically performing this action is the expected method of preventing the watchdog from timing out (and resetting the MCU).	32	wo	0x0

8.2.6.4 CNTVAL

0x5001030C CNTVAL ^

Counter value.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset

F0	CNTVAL	Counter value. The instantaneous value of watchdog timeout counter	32	ro	0x0

8.2.6.5 INT

0x50010310 **INT** ^

WDTA Interrupts. Contains the ENABLE, CLEAR, STATUS and IRQ.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						F25	F24							F17	F16	-						F9	F8	-						F1	F0

#	Field Name	Field Description	Width	Access	Reset
F25	WINOPEN	Window Open Interrupt. Set by WDTA timeout	1	ro	0x0
F24	WDTA	WDTA timeout Interrupt. Set by WDTA timeout	1	ro	0x0
F17	WINOPEN	Window Open Status. Set by WDTA timeout	1	ro	0x0
F16	WDTA	WDTA timeout Status. Set by WDTA timeout	1	ro	0x0
F9	WINOPEN	Window Open Interrupt Clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F8	WDTA	WDTA timeout Interrupt Clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F1	WINOPEN	Window Open Interrupt Enable.	1	rw	0x0
F0	WDTA	WDTA timeout Interrupt Enable.	1	rw	0x0

8.2.7 Pulse width modulation

PWM		
Address	**Register Name**	**Description**
0x50010600	BASE	Base functions
0x50010604	PWMCNT	PWM Count Value
0x50010608	ENAREQ	Enable request
0x5001060C	ENASTS	Enable status
0x50010610	INIT	Initial State of Outputs
0x50010614	INV	Invert
0x50010618	UPDATE	Update
0x5001061C	PULSE0	PWM0 pulse setup
0x50010620	PULSE1	PWM1 pulse setup
0x50010624	PULSE2	PWM2 pulse setup
0x50010628	INTPOSEDGENA	PWM posedge interrupt enable
0x5001062C	INTNEGEDGENA	PWM negedge interrupt enable
0x50010630	INTPOSEDGCLR	PWM posedge interrupt control
0x50010634	INTNEGEDGCLR	PWM negedge interrupt control
0x50010638	INTPOSEDGSTS	PWM posedge interrupt status
0x5001063C	INTNEGEDGSTS	PWM negedge interrupt status

0x50010640	INTPOSEDGIRQ	PWM posedge interrupt active
0x50010644	INTNEGEDGIRQ	PWM negedge interrupt active
0x50010648	INTPWM	PWM interrupt control

8.2.7.1 BASE

0x50010600 BASE ^

Base functions.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																-	-	-	-	-	F8			-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F16	PERIOD	Period. Specifies the period of the output waveform in terms of a number of prescaler output cycles.	16	rw	0x0
F8	PRESCALESEL	Prescaler select. Defines the ratio between the system clock and the clock used for the waveform generator. 0x0: Divide by 1 0x1: Divide by 2 0x2: Divide by 4 0x3: Divide by 8 0x4: Divide by 16 0x5: Divide by 64 0x6: Divide by 256 0x7: Divide by 1024	3	rw	0x0

8.2.7.2 PWMCNT

0x50010604 PWMCNT ^

PWM Count Value.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	PWMCNT	PWM counter value to give a sense about the current period	16	dual	0x0

8.2.7.3 ENAREQ

0x50010608 **ENAREQ** ^

Enable request.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	F26	F25	F24	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F26	FORCEINACTIVE	Set to force PWM signals return to initial value immediately.	1	rw	0x0
F25	CLRREQALL	Write 1 to clear all ENA_REQ bits; Write 0 has no effects.	1	wo	0x0
F24	ENAREQALL	Write 1 to enable all ENA_REQ bits; Write 0 has no effects.	1	wo	0x0
F0	ENAREQ	Set to enable the waveform generator.	3	rw	0x0

8.2.7.4 ENASTS

0x5001060C **ENASTS** ^

Enable status.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F0	ENASTS	Status of enable in the waveform generator.	3	ro	0x0

8.2.7.5 INIT

0x50010610	INIT	^

Intial State of Outputs.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F0	INIT	Set to initialise the output waveform.	3	rw	0x0

8.2.7.6 INV

0x50010614	INV	^

Invert.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F0	INVERT	Set to invert the output waveform.	3	rw	0x0

8.2.7.7 UPDATE

0x50010618	UPDATE	^

Update.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	UPDATE	Set to trigger consumption of new PULSE parameters (invert,prescale_sel,period,pulse start & stop). The flag is automatically cleared by the hardware when the settings are consumed, so reading a high value indicates that an update is still pending.	1	dual	0x0

8.2.7.8 PULSE0

0x5001061C **PULSE0** ^

PWM0 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE0	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL0	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

8.2.7.9 PULSE1

0x50010620 **PULSE1** ^

PWM1 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE1	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL1	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

8.2.7.10 PULSE2

0x50010624	PULSE2	^

PWM2 pulse setup.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F16																F0															

#	Field Name	Field Description	Width	Access	Reset
F16	PRISE2	Pulse Rise. Specifies the pulse rise of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse fall timing.	16	rw	0x0
F0	PFALL2	Pulse Fall. Specifies the pulse fall of the output waveform in terms of a number of prescaler output cycles. However, if INVERT is set it determines the pulse rise timing.	16	rw	0x0

8.2.7.11 INTPOSEDGENA

0x50010628	INTPOSEDGENA	^

PWM posedge interrupt enable. Contains the enable for the PWM posedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F0	INTPOSEDGENA	Interrupt enable. bit[2:0]: posedge interrupt enable.	3	rw	0x0

8.2.7.12 INTNEGEDGENA

0x5001062C	INTNEGEDGENA	^

PWM negedge interrupt enable. Contains the enable for the PWM negedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F0	INTNEGEDGENA	Interrupt enable. bit[2:0]: negedge interrupt enable.	3	rw	0x0

8.2.7.13 INTPOSEDGCLR

0x50010630	INTPOSEDGCLR	^

PWM posedge interrupt control. Contains the clear for the PWM posedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset

F0	INTPOSEDGCLR	Interrupt clear. bit[2:0] : posedge interrupt clear.	3	wo	0x0

8.2.7.14 INTNEGEDGCLR

0x50010634 INTNEGEDGCLR ^

PWM negedge interrupt control. Contains the clear for the PWM negedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F0	INTNEGEDGCLR	Interrupt clear. bit[2:0] : negedge interrupt clear.	3	wo	0x0

8.2.7.15 INTPOSEDGSTS

0x50010638 INTPOSEDGSTS ^

PWM posedge interrupt status. Contains the status for the PWM posedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F0	INTPOSEDGSTS	Interrupt status. bit[2:0] : posedge interrupt status.	3	ro	N/A

8.2.7.16 INTNEGEDGSTS

0x5001063C INTNEGEDGSTS ^

PWM negedge interrupt status. Contains the status for the PWM negedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F0	INTNEGEDGSTS	Interrupt status. bit[2:0] : negedge interrupt status.	3	ro	N/A

8.2.7.17 INTPOSEDGIRQ

0x50010640 **INTPOSEDGIRQ** ^

PWM posedge interrupt active. Contains the active for the PWM posedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F0	INTPOSEDGIRQ	Interrupt active. bit[2:0] : posedge interrupt active.	3	ro	N/A

8.2.7.18 INTNEGEDGIRQ

0x50010644 **INTNEGEDGIRQ** ^

PWM negedge interrupt active. Contains the active for the PWM negedge interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0		

#	Field Name	Field Description	Width	Access	Reset
F0	INTNEGEDGIRQ	Interrupt active. bit[2:0] : negedge interrupt active.	3	ro	N/A

8.2.7.19 INTPWM

0x50010648 **INTPWM** ^

PWM interrupt control. Contains the enable, clear, status and active for the PWM period & updated interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	F25	F24	-	-	-	-	-	-	F17	F16	-	-	-	-	-	-	F9	F8	-	-	-	-	-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F25	UPD	Updated Interrupt active.	1	ro	N/A
F24	PERIOD	Period Interrupt active.	1	ro	N/A
F17	UPD	Updated Interrupt status.	1	ro	N/A
F16	PERIOD	Period Interrupt status.	1	ro	N/A
F9	UPD	Updated Interrupt clear.	1	wo	0x0
F8	PERIOD	Period Interrupt clear.	1	wo	0x0
F1	UPD	Updated Interrupt enable.	1	rw	0x0
F0	PERIOD	Period Interrupt enable.	1	rw	0x0

8.2.8 LIN Slave Controller

LINS		
Address	**Register Name**	**Description**
0x50010700	DATABYTE1	Data Byte 1
0x50010704	DATABYTE2	Data Byte 2
0x50010708	DATABYTE3	Data Byte 3
0x5001070C	DATABYTE4	Data Byte 4

0x50010710	DATABYTE5	Data Byte 5
0x50010714	DATABYTE6	Data Byte 6
0x50010718	DATABYTE7	Data Byte 7
0x5001071C	DATABYTE8	Data Byte 8
0x50010720	CTRL	Control Register
0x50010724	STATUS	Status
0x50010728	ERROR	Error Register
0x5001072C	DL	DATA Length Register
0x50010730	BTDIV07	Bit time Divider Register
0x50010734	BITTIME	Control Settings
0x50010738	ID	ID Register
0x5001073C	BUSTIME	Lin Bus Timing Register
0x50010740	STATUSEXT	Extended Status
0x50010744	WUPDETECTTHRES	Wakeup Detection Threshold

8.2.8.1 DATABYTE1

0x50010700	DATABYTE1	^

Data Byte 1.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	DATABUF1	Data Buffer 1. 1st byte of the 8-byte Data Buffer	8	rw	0x0

8.2.8.2 DATABYTE2

0x50010704 DATABYTE2 ^

Data Byte 2.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	DATABUF2	Data Buffer 2. 2nd byte of the 8-byte Data Buffer	8	rw	0x0

8.2.8.3 DATABYTE3

0x50010708 DATABYTE3 ^

Data Byte 3.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	DATABUF3	Data Buffer 3. 3rd byte of the 8-byte Data Buffer	8	rw	0x0

8.2.8.4 DATABYTE4

0x5001070C	DATABYTE4	^

Data Byte 4.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	DATABUF4	Data Buffer 4. 4th byte of the 8-byte Data Buffer	8	rw	0x0

8.2.8.5 DATABYTE5

0x50010710	DATABYTE5	^

Data Byte 5.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	DATABUF5	Data Buffer 5. 5th byte of the 8-byte Data Buffer	8	rw	0x0

8.2.8.6 DATABYTE6

0x50010714	DATABYTE6	^

Data Byte 6.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	DATABUF6	Data Buffer 6. 6th byte of the 8-byte Data Buffer	8	rw	0x0

8.2.8.7 DATABYTE7

0x50010718 **DATABYTE7** ^

Data Byte 7.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	DATABUF7	Data Buffer 7. 7th byte of the 8-byte Data Buffer	8	rw	0x0

8.2.8.8 DATABYTE8

0x5001071C **DATABYTE8** ^

Data Byte 8.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	DATABUF8	Data Buffer 8. 8th byte of the 8-byte Data Buffer	8	rw	0x0

8.2.8.9 CTRL

0x50010720	CTRL	^
Control Register.		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F7	F6	F5	F4	F3	F2	F1	-

#	Field Name	Field Description	Width	Access	Reset
F7	STOP	Stop Register. The host controller of the LIN slave has set this register if it handles a data request interrupt and can not make use of the frame content with the received identifier(e.g. extended identifiers). For that case the LIN slave stops the processing of the LIN communication until the next SYNC BREAK is detected. A read access to this bit delivers always the value 0	1	wo	0x0
F6	SLEEP	Sleep Request. The bit is used by the LIN core to determine whether the LIN bus is in Sleep Mode or not. The host controller has to set the bit after sending or receiving a Sleep Mode frame The bit will be set automatically by the LIN core if a bus idle timeout is detected. The host controller has to clear the bit after a wakeup signal is detected.	1	rw	0x0
F5	TRANSMIT	Transmit Operation. The bit determines whether the current frame is a transmit frame or a receive frame for the LIN node. It has to be set by the host controller. 0x0: receive operation 0x1: transmit operation	1	rw	0x0
F4	DATAACK	Data Acknowledgement. The bit has to be set by the host controller of a LIN slave after handling a data request interrupt (compare STATUS.DATA_REQ register). The bit will be reset by the LIN core.	1	rw	0x0

F3	RSTINT	Reset interrupt. The host controller has to set this bit to reset the STATUS.INTR register and the interrupt request output of the LIN core. A read access to this bit delivers always the value 0.	1	wo	0x0
F2	RSTERR	Reset Error. The host controller has to set this bit to reset the error bits in status register and error register. A read access to this bit delivers always the value 0.	1	wo	0x0
F1	WAKEUPREQ	WakeUp Request. The bit has to be set by the host controller to terminate the Sleep Mode of the LIN bus by sending a Wakeup signal. The bit will be reset by the LIN core.	1	rw	0x0

8.2.8.10 STATUS

0x50010724 **STATUS** ^

Status.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F7	F6	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F7	ACTIVE	Lin Bus Active. The bit indicates whether the LIN bus is active or not. Note: For the LIN slave, this bit is set after the detection of a correct SYNC BREAK / SYNC FIELD sequence and it is reset at the end of the transmission or if the processing of the current frame is stopped by the host controller 0x0: no Lin bus activity 0x1: transmission on the LIN bus is active	1	ro	0x0
F6	BUSIDLETIMEOUT	BUS Idle Timeout. This bit is set by the LIN core if LIN is in hardware mode and no bus activity is detected for 4s~10s. In addition, an interrupt request to the host controller is generated in that case. After that, It is assumed that the LIN bus is in sleep mode and CTRL.SLEEP register will be set by the LIN core. The bit has to be reset by the host controller by setting the bit CTRL.RST_INT register.	1	ro	0x0
F5	ABORTED	Aborted. The bit is set if the processing of the current frame has been stopped by setting CTRL.STOP register.	1	ro	0x0

		The bit is cleared by the LIN core after receiving a correct SYNC BREAK / SYNC FIELD sequence			
F4	DATAREQ	Data Request. The LIN core slave sets the bit after receiving the Identifier and requests an interrupt to the host controller. The host controller has to decode the Identifier to decide whether the current frame is a transmit or a receive operation. It has to adjust CTRL.TRANSMIT register and to load the data length. For transmit operations it has to load the data buffer too. After that the host controller has to set CTRL.DATA_ACK register	1	ro	0x0
F3	INTR	Interupt Request. The LIN core sets the bit when it requests an interrupt to the host controller. It has the same value as the interrupt output INTR. The bit has to be reset by the host controller by setting the bit CTRL.RST_INT register	1	ro	0x0
F2	ERROR	Lin Error. The LIN core sets the bit if an error has been detected (compare error register). The bit has to be reset by the host controller by setting the bit CTRL.RST_ERR register	1	ro	0x0
F1	WAKEUP	WakeUp. The bit is set when the LIN core is transmitting a Wakeup signal.	1	ro	0x0
F0	COMPLETE	Complete. The LIN core will set the bit after a transmission has been successfully finished and it will reset it at the start of a transmission	1	ro	0x0

8.2.8.11 ERROR

0x50010728	ERROR	^

Error Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F6	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset

F6	FRAMEERR	Byte Field Framing Error. This bit is set by the LIN core slave if a transmission is aborted after the beginning of the data field due to a timeout or an incomplete frame	1	ro	0x0
F5	SBITERR	Start Bit Error in Byte field. Start Bit Error in Byte field, i.e., invalid start bit.	1	ro	0x0
F4	BITMON	Bit Monitor Error. The Bit value monitored on the bus is different from the sent bit value	1	ro	0x0
F3	PARITY	Parity Error. Identifier parity error	1	ro	0x0
F2	TIMEOUT	Timeout Error. There are several reason that can cause a timeout error: The master detects a timeout error if it is expecting data from the bus but no slave does respond. If the slave responds to late and the frame is not finished within the maximum frame length TFRAME_MAX a timeout error will be detected too. The slave detects a timeout error if it is requesting a data acknowledge to the host controller (for selecting receive or transmit, data length and loading data), and the host controller does not set CTRL.DATA_ACK or CTRL.STOP register until the end of the reception of the first byte after the identifier. The slave detects a timeout error if it has transmitted a wakeup signal and it detects no sync field (from the master) within 150 ms. Note: The slave does not perform an exact check of the frame length TFRAME_MAX but a timeout is detected after 200 bit times, if the slave is in receive mode and there are missing data fields or a missing ID field from the master.	1	ro	0x0
F1	CHK	Checksum Error. Checksum Error	1	ro	0x0
F0	BITERR	Bit Error in Byte field. Bit Error in Byte field, i.e., invalid stop bit.	1	ro	0x0

8.2.8.12 DL

0x5001072C	DL	^
DATA Length Register.		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F7	F6	-	-	F0			

#	Field Name	Field Description	Width	Access	Reset
F7	ENHCHK	Enhancement Check. The host controller has to set the checksum type used in the current frame by adjusting this register. 0x0: for classic checksum 0x1: for enhanced checksum	1	rw	0x0
F6	DISBITMON	Disable Bit Monitor. Set to disable the bit monitor during transmission. The bit must be set in case that RXD/TXD are separated.	1	rw	0x0
F0	LENGTH	Data Length. The host controller has to define the length of the data field of the current LIN frame by adjusting the data length register. If the data length is loaded with the value 1111b the length of the data field is decoded from Bit 5 and 4 of the identifier register id according to the Table below (e.g. compatibility to LIN specification 1.1). Otherwise the amount of data bytes can be written directly to the data length register (supported values are 0..8).	4	rw	0x0

ID (Bit 5)	ID (Bit 4)	Number of Bytes in the data field
0	0	2
0	1	2
1	0	4
1	1	8

8.2.8.13 BTDIV07

0x50010730	BTDIV07	^

Bit time Divider Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	BTDIV07	Bt Div LSBs. Bit time divider [7:0]	8	rw	0xFF

8.2.8.14 BITTIME

0x50010734	BITTIME	^

Control Settings.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F6		-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F6	PRESCL	Prescaler Register. Prescaler Setting	2	rw	0x3
F0	BTDIV8	Bt Div Most Significant bit. Bit time divider [8]	1	rw	0x1

8.2.8.15 ID

0x50010738	ID	^

ID Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0					

#	Field Name	Field Description	Width	Access	Reset
F0	ID	ID. ID register	6	rw	0x0

8.2.8.16 BUSTIME

0x5001073C **BUSTIME** ^

Lin Bus Timing Register. Table 2-9 Control of time settings for wup_repeat_time and bus_inactivity_time

Bit 3	Bit 2	Bit 1	Bit 0	Time
0	0	0	0	Reset value
0	0			4 s (bus_inactivity_time)
0	1			6 s (bus_inactivity_time)
1	0			8 s (bus_inactivity_time)
1	1			10 s (bus_inactivity_time)
		0	0	180 ms (wup_repeat_time)
		0	1	200 ms (wup_repeat_time)
		1	0	220 ms (wup_repeat_time)
		1	1	240 ms (wup_repeat_time)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F4	F2		F0	

#	Field Name	Field Description	Width	Access	Reset

F4	BUSDOMINANTRELEASEWUPENA	Bus Dominant Release Wakeup Enable.	1	rw	0x0
F2	BUSINACTIVE	Bus Inactivity Time.	2	rw	0x0
F0	WUPREPEAT	wakeup repeat time.	2	rw	0x0

8.2.8.17 STATUSEXT

0x50010740 STATUSEXT ^

Extended Status.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F2		F1	F0

#	Field Name	Field Description	Width	Access	Reset
F2	BUSIDLEMONITOR	Bus Idle Monitor Status. If LIN is in hardware mode, BIT[0] is set by the lin core if the bus has no activity for 4s~10s and BIT[1] is set by the lin core if LIN is stuck at dominant inactivity state for 4s~10s. Any bus transition will clear these two bits. LIN Slave's pullup will be disabled & LIN Master's pullup will be reduced to 30K when BIT[1] is set.	2	ro	0x0
F1	BUSIDLETIMEOUTDOMINANT	Dominant Bus Idle Timeout. The bit is set by the lin core if LIN is in hardware mode & the bus is stuck at dominant inactivity state for 4s~10s. The bit has to be reset by the host controller by setting the bit CTRL.RST_INT register.	1	ro	0x0
F0	COMPLETETX	Complete TX. The LIN core will set the bit after a TX transmission has been successfully finished and it will reset it at the start of a transmission.	1	ro	0x0

8.2.8.18 WUPDETECTTHRES

0x50010744	WUPDETECTTHRES	^

Wakeup Detection Threshold.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0					

#	Field Name	Field Description	Width	Access	Reset
F0	WUPDETECTTHRES	Wakeup Detection Threshold. Threshold setting(LF_CLK_PREDIV clock cycls) of lin wakeup signal. Only take effect when CLK_LF_SEL = 1; For instace, if target threshold is 150us@LF_CLK_PREDIV=256KHz, WUP_DETECT_THRES = 150/(1000/256)+1.	6	rw	0x29

8.2.9 LIN Master Controller

LINM		
Address	**Register Name**	**Description**
0x50010800	DATABYTE1	Data Byte 1
0x50010804	DATABYTE2	Data Byte 2
0x50010808	DATABYTE3	Data Byte 3
0x5001080C	DATABYTE4	Data Byte 4
0x50010810	DATABYTE5	Data Byte 5

0x50010814	DATABYTE6	Data Byte 6
0x50010818	DATABYTE7	Data Byte 7
0x5001081C	DATABYTE8	Data Byte 8
0x50010820	CTRL	Control Register
0x50010824	STATUS	Status
0x50010828	ERROR	Error Register
0x5001082C	DL	DATA Length Register
0x50010830	BTDIV07	Bit time Divider Register
0x50010834	BITTIME	Control Settings
0x50010838	ID	ID Register
0x5001083C	BUSTIME	Lin Bus Timing Register
0x50010840	STATUSEXT	Extended Status
0x50010844	WUPDETECTTHRES	Wakeup Detection Threshold

8.2.9.1 DATABYTE1

0x50010800	DATABYTE1	^

Data Byte 1.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset

F0	DATABUF1	Data Buffer 1. 1st byte of the 8-byte Data Buffer	8	rw	0x0

8.2.9.2 DATABYTE2

0x50010804 DATABYTE2 ^

Data Byte 2.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	DATABUF2	Data Buffer 2. 2nd byte of the 8-byte Data Buffer	8	rw	0x0

8.2.9.3 DATABYTE3

0x50010808 DATABYTE3 ^

Data Byte 3.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	DATABUF3	Data Buffer 3. 3rd byte of the 8-byte Data Buffer	8	rw	0x0

8.2.9.4 DATABYTE4

0x5001080C	DATABYTE4	^

Data Byte 4.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	DATABUF4	Data Buffer 4. 4th byte of the 8-byte Data Buffer	8	rw	0x0

8.2.9.5 DATABYTE5

0x50010810	DATABYTE5	^

Data Byte 5.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	DATABUF5	Data Buffer 5. 5th byte of the 8-byte Data Buffer	8	rw	0x0

8.2.9.6 DATABYTE6

0x50010814	DATABYTE6	^

Data Byte 6.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	DATABUF6	Data Buffer 6. 6th byte of the 8-byte Data Buffer	8	rw	0x0

8.2.9.7 DATABYTE7

0x50010818 **DATABYTE7** ^

Data Byte 7.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	DATABUF7	Data Buffer 7. 7th byte of the 8-byte Data Buffer	8	rw	0x0

8.2.9.8 DATABYTE8

0x5001081C **DATABYTE8** ^

Data Byte 8.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	DATABUF8	Data Buffer 8. 8th byte of the 8-byte Data Buffer	8	rw	0x0

8.2.9.9 CTRL

0x50010820	CTRL	^

Control Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F7	F6	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F7	STOP	Stop Register. The host controller of the LIN slave has set this register if it handles a data request interrupt and can't make use of the frame content with the received identifier (e.g. extended identifiers). For that case the LIN slave stops the processing of the LIN communication until the next SYNC BREAK is detected. A read access to this bit delivers always the value 0.	1	wo	0x0
F6	SLEEP	Sleep Request. The bit is used by the LIN core to determine whether the LIN bus is in Sleep Mode or not. The host controller has to set the bit after sending or receiving a Sleep Mode frame. The bit will be set automatically by the LIN core if a bus idle timeout is detected. The host controller has to clear the bit after a wakeup signal is detected.	1	rw	0x0
F5	TRANSMIT	Transmit Operation. The bit determines whether the current frame is a transmit frame or a receive frame for the LIN node. It has to be set by the host controller. 0x0: receive operation 0x1: transmit operation	1	rw	0x0
F4	DATAACK	Data Acknowledgement. The bit has to be set by the host controller of a LIN slave after handling a data request interrupt (compare STATUS.DATA_REQ register). The bit will be reset by the LIN core.	1	rw	0x0
F3	RSTINT	Reset interrupt. The host controller has to set this bit to reset the STATUS.INTR register and the interrupt request output of the LIN core. A read access to this bit delivers always the value 0.	1	wo	0x0

F2	RSTERR	Reset Error. The host controller has to set this bit to reset the error bits in status register and error register. A read access to this bit delivers always the value 0.	1	wo	0x0
F1	WAKEUPREQ	WakeUp Request. The bit has to be set by the host controller to terminate the Sleep Mode of the LIN bus by sending a Wakeup signal. The bit will be reset by the LIN core.	1	rw	0x0
F0	STARTREQ	Start Request. The bit has to be set by the host controller of a LIN master to start the LIN transmission after loading identifier,data length and data buffer. The bit will be reset by the LIN core after the transmission is finished or an error is occurred.	1	rw	0x0

8.2.9.10 STATUS

0x50010824	STATUS	^

Status.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F7	F6	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F7	ACTIVE	Lin Bus Active. The bit indicates whether the LIN bus is active or not. Note: For the LIN slave, this bit is set after the detection of a correct SYNC BREAK / SYNC FIELD sequence and it is reset at the end of the transmission or if the processing of the current frame is stopped by the host controller 0x0: no Lin bus activity 0x1: transmission on the LIN bus is active	1	ro	0x0
F6	BUSIDLETIMEOUT	BUS Idle Timeout. This bit is set by the LIN core if LIN is in hardware mode and no bus activity is detected for 4s~10s. In addition, an interrupt request to the host controller is generated in that case. After that, It is assumed that the LIN bus is in sleep mode and CTRL.SLEEP register will be set by the LIN core. The bit	1	ro	0x0

		has to be reset by the host controller by setting the bit CTRL.RST_INT register.			
F5	ABORTED	Aborted. The bit is set if the processing of the current frame has been stopped by setting CTRL.STOP register. The bit is cleared by the LIN core after receiving a correct SYNC BREAK / SYNC FIELD sequence	1	ro	0x0
F4	DATAREQ	Data Request. The LIN core slave sets the bit after receiving the Identifier and requests an interrupt to the host controller. The host controller has to decode the Identifier to decide whether the current frame is a transmit or a receive operation. It has to adjust CTRL.TRANSMIT register and to load the data length. For transmit operations it has to load the data buffer too. After that the host controller has to set CTRL.DATA_ACK register	1	ro	0x0
F3	INTR	Interupt Request. The LIN core sets the bit when it requests an interrupt to the host controller. It has the same value as the interrupt output INTR. The bit has to be reset by the host controller by setting the bit CTRL.RST_INT register	1	ro	0x0
F2	ERROR	Lin Error. The LIN core sets the bit if an error has been detected (compare error register). The bit has to be reset by the host controller by setting the bit CTRL.RST_ERR register	1	ro	0x0
F1	WAKEUP	WakeUp. The bit is set when the LIN core is transmitting a Wakeup signal.	1	ro	0x0
F0	COMPLETE	Complete. The LIN core will set the bit after a transmission has been successfully finished and it will reset it at the start of a transmission	1	ro	0x0

8.2.9.11 ERROR

0x50010828	ERROR	^

Error Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F6	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F6	FRAMEERR	Byte Field Framing Error. This bit is set by the LIN core slave if a transmission is aborted after the beginning of the data field due to a timeout or an incomplete frame	1	ro	0x0
F5	SBITERR	Start Bit Error in Byte field. Start Bit Error in Byte field, i.e., invalid start bit.	1	ro	0x0
F4	BITMON	Bit Monitor Error. The Bit value monitored on the bus is different from the sent bit value	1	ro	0x0
F3	PARITY	Parity Error. Identifier parity error	1	ro	0x0
F2	TIMEOUT	Timeout Error. There are several reason that can cause a timeout error: The master detects a timeout error if it is expecting data from the bus but no slave does respond. If the slave responds to late and the frame is not finished within the maximum frame length TFRAME_MAX a timeout error will be detected too. The slave detects a timeout error if it is requesting a data acknowledge to the host controller (for selecting receive or transmit, data length and loading data), and the host controller does not set CTRL.DATA_ACK or CTRL.STOP register until the end of the reception of the first byte after the identifier. The slave detects a timeout error if it has transmitted a wakeup signal and it detects no sync field (from the master) within 150 ms. Note: The slave does not perform an exact check of the frame length TFRAME_MAX but a timeout is detected after 200 bit times, if the slave is in receive mode and there are missing data fields or a missing ID field from the master.	1	ro	0x0
F1	CHK	Checksum Error. Checksum Error	1	ro	0x0
F0	BITERR	Bit Error in Byte field. Bit Error in Byte field, i.e., invalid stop bit.	1	ro	0x0

8.2.9.12 DL

0x5001082C	DL	^

DATA Length Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F7	F6	-	-	F0			

#	Field Name	Field Description	Width	Access	Reset
F7	ENHCHK	Enhancement Check. The host controller has to set the checksum type used in the current frame by adjusting this register. 0x0: for classic checksum 0x1: for enhanced checksum	1	rw	0x0
F6	DISBITMON	Disable Bit Monitor. Set to disable the bit monitor during transmission. The bit must be set in case that RXD/TXD are separated.	1	rw	0x0
F0	LENGTH	Data Length. The host controller has to define the length of the data field of the current LIN frame by adjusting the data length register. If the data length is loaded with the value 1111b the length of the data field is decoded from Bit 5 and 4 of the identifier register id according to the Table below (e.g. compatibility to LIN specification 1.1). Otherwise the amount of data bytes can be written directly to the data length register (supported values are 0..8).	4	rw	0x0

ID (Bit 5)	ID (Bit 4)	Number of Bytes in the data field
0	0	2
0	1	2
1	0	4
1	1	8

8.2.9.13 BTDIV07

0x50010830	BTDIV07	^

Bit time Divider Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	BTDIV07	Bt Div LSBs. Bit time divider [7:0]	8	rw	0xFF

8.2.9.14 BITTIME

0x50010834	BITTIME	^

Control Settings.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F6		F1					F0

#	Field Name	Field Description	Width	Access	Reset
F6	PRESCL	Prescaler Register. Prescaler Setting	2	rw	0x3
F1	BTMULT	Bt Div Most Significant bit. Bit time multiplier [4:0]	5	rw	0x1
F0	BTDIV8	Bt Div Most Significant bit. Bit time divider [8]	1	rw	0x1

8.2.9.15 ID

0x50010838	ID	^

ID Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0					

#	Field Name	Field Description	Width	Access	Reset
F0	ID	ID. ID register	6	rw	0x0

8.2.9.16 BUSTIME

0x5001083C **BUSTIME** ^

Lin Bus Timing Register. Table 2-9 Control of time settings for wup_repeat_time and bus_inactivity_time

Bit 3	Bit 2	Bit 1	Bit 0	Time
0	0	0	0	Reset value
0	0			4 s (bus_inactivity_time)
0	1			6 s (bus_inactivity_time)
1	0			8 s (bus_inactivity_time)
1	1			10 s (bus_inactivity_time)
		0	0	180 ms (wup_repeat_time)
		0	1	200 ms (wup_repeat_time)
		1	0	220 ms (wup_repeat_time)
		1	1	240 ms (wup_repeat_time)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F4	F2	F0

#	Field Name	Field Description	Width	Access	Reset
F4	BUSDOMINANTRELEASEWUPENA	Bus Dominant Release Wakeup Enable.	1	rw	0x0
F2	BUSINACTIVE	Bus Inactivity Time.	2	rw	0x0
F0	WUPREPEAT	wakeup repeat time.	2	rw	0x0

8.2.9.17 STATUSEXT

0x50010840 **STATUSEXT** ^

Extended Status.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F2		F1	F0

#	Field Name	Field Description	Width	Access	Reset
F2	BUSIDLEMONITOR	Bus Idle Monitor Status. If LIN is in hardware mode, BIT[0] is set by the lin core if the bus has no activity for 4s~10s and BIT[1] is set by the lin core if LIN is stuck at dominant inactivity state for 4s~10s. Any bus transition will clear these two bits. LIN Slave's pullup will be disabled & LIN Master's pullup will be reduced to 30K when BIT[1] is set.	2	ro	0x0
F1	BUSIDLETIMEOUTDOMINANT	Dominant Bus Idle Timeout. The bit is set by the lin core if LIN is in hardware mode & the bus is stuck at dominant inactivity state for 4s~10s. The bit has to be reset by the host controller by setting the bit CTRL.RST_INT register.	1	ro	0x0
F0	COMPLETETX	Complete TX. The LIN core will set the bit after a TX transmission has been successfully finished and it will reset it at the start of a transmission.	1	ro	0x0

8.2.9.18 WUPDETECTTHRES

0x50010844	WUPDETECTTHRES	^

Wakeup Detection Threshold.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0					

#	Field Name	Field Description	Width	Access	Reset
F0	WUPDETECTTHRES	Wakeup Detection Threshold. Threshold setting(LF_CLK_PREDIV clock cycls) of lin wakeup signal. Only take effect when CLK_LF_SEL = 1; For instace, if target threshold is 150us@LF_CLK_PREDIV=256KHz, WUP_DETECT_THRES = 150/(1000/256)+1.	6	rw	0x29

8.2.10 ADC Controller

ADC		
Address	**Register Name**	**Description**
0x50010D00	CONF	configuration settings for the ADC
0x50010D04	CNTRL	ADC Data Conversion Control Register
0x50010D08	TSET	Settling Time settings Register
0x50010D0C	DATA1	Data Out of CH1,
0x50010D10	DATA2	Data Out of CH2,

0x50010D14	DATA0345	Data Out of CH0/CH3/CH4/CH5,
0x50010D18	STATUS	Status Register,

8.2.10.1 CONF

0x50010D00 CONF ^

configuration settings for the ADC. set this up before starting a conversion.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	F16							-	-	-	-	F8				-	F6	-	-	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F16	SAMPCYC	Sample cycle. setting sampling time to SAMPCYC+2 adc clock cycle, where adc clock cycle is system clock divide by 4. For LED measure(adc channel2), adc sample cycle need >= 2us; for non-LED measure(other channel), adc sample cycle need >= 8us	7	rw	0x8
F8	SYNCENA	Sync Enable. Need to set this bit if the conversion needs to be in sync with an sync input 0x1: Triggered by the posedge of the pwm signal. 0x2: Triggered by the negedge of the pwm signal. 0x4: Triggered by the period pulse of pwm. 0x8: Triggered by Soft Sync Input.	4	rw	0x0
F6	SWSYNCIN	Soft Sync Input. Write 1 to trigger an adc conversion if SYNC_ENA[3] = 1; This register will be used mainly for debug purpose with hw sync disabled we can emulate the hw sync signal in this register	1	wo	0x0
F3	BIASENA	ADC Bias Enable. Set to enable ADC Bias when the chip is active, otherwise ADC bias is only enabled during conversion.	1	rw	0x0
F2	ATTEN	ADC input Attenuation setting. if set ADC will convert Vin/3	1	rw	0x0

F1	AUTOEN	Bias Enable mode. 0x0: Bias is Enabled Continuously 0x1: Bias is Enabled only after strb	1	rw	0x0
F0	MODE	ADC mode select. Selects the ADC operating mode. 0x0: Diffrential Mode A/D Conversion 0x1: Single Mode A/D Conversion	1	rw	0x1

8.2.10.2 CNTRL

0x50010D04 **CNTRL** ^

ADC Data Conversion Control Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	F26			F24		-	-	-	-	F18		F16		-	-	F8						F7	F6	F4		-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F26	CH4SEL	Channel4 Selection. Selects the analog outputs of GPIO1~5 connected to CH4 0x0: GPIO1 connected to CH4 0x1: GPIO2 connected to CH4 0x2: GPIO3 connected to CH4 0x3: GPIO4 connected to CH4 0x4: GPIO5 connected to CH4 0x5: GPIO6 connected to CH4	3	rw	0x0
F24	CH3SEL	Channel3 Selection. Channel3 Selects. 0x0: Accurate VBAT(1/32) 0x1: GPIO3 0x2: Internal Temperature sensor 0x3: GPIO4	2	rw	0x2
F18	CH2SEL	Channel2 Selection. Selects the forward voltage of the external LEDs connected to CH2; The selected LED CH_NO = CH2_SEL.	2	rw	0x0
F16	CH1SEL	Channel1 Selection. Channel1 Selects. 0x0: Accurate VBAT(1/32)	2	rw	0x1

		0x1: GPIO1 0x2: Internal Temperature sensor 0x3: GPIO2			
F8	CHSEQ	Channel Sequence. Selects the sequence of channels to be converted CH0: Buffered bandgap voltage CH1: Accurate VBAT(1/32)/GPIO1/Internal Temperature sensor/GPIO2 CH2: VFW(The forward voltage of the external LEDs), same as (VDD5V-VLED)/4. CH3: Accurate VBAT(1/32)/GPIO3/Internal Temperature sensor/GPIO4 CH4: analog port of GPIO1~6 CH5: VDD1V5 0x0: Only CH0 0x1: Only CH1 0x2: Only CH2 0x4: Only CH3 0x8: Only CH4 0x10: Only CH5 0x21: CH1 followed by CH2 0x29: CH1 followed by CH3 0x22: CH2 followed by CH3 0x2a: CH2 followed by CH1 0x24: CH3 followed by CH1 0x2c: CH3 followed by CH2 0x31: CH1 followed by CH2 followed by CH3 0x39: CH1 followed by CH3 followed by CH2 0x32: CH2 followed by CH3 followed by CH1 0x3a: CH2 followed by CH1 followed by CH3 0x34: CH3 followed by CH1 followed by CH2 0x3c: CH3 followed by CH2 followed by CH1	6	rw	0x3F
F7	IRQCLR	IRQ Clear.	1	wo	0x0
F6	IRQENA	IRQ Enable.	1	rw	0x0
F4	STUPDLY	Startup Delay. Delay between adc getting enabled and the 1st strbi(command to start a conversion) 0x0: 1us Delay 0x1: 8us Delay 0x2: 12us Delay 0x3: 16us Delay	2	rw	0x2
F1	CONT	Continuous Convesion Enable. if set enables the continuous conversion mode, else it's a single conversion. This is only checked at the end of current conversion	1	rw	0x0
F0	CONVERT	ADC START/STATUS Register. Set to start a conversion, gets cleared at the end of single conversion. If CONT is set then this doesn't get cleared at the end of	1	rw	0x0

		conversion. This can be read to check the current status of ADC conversion.			

8.2.10.3 TSET

0x50010D08	TSET	^

Settling Time settings Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F8				F4				F0			

#	Field Name	Field Description	Width	Access	Reset
F8	TGUARD	TGUARD setting. It's the guard time where there is no channel is selected, while switching from one channel in the sequence to the other to avoid any overlap. Guard Time = (TGUARD+1)x 250ns	4	rw	0x3
F4	TCHNL	TCHNL setting. It's the time to wait after the guard time for the conversions of 2nd or 3rd channel in the sequence, to allow settling of the channel before start of the conversion Channel Time = (TCHNL+1)x 250ns	4	rw	0x0
F0	TCURR	TCURR setting. if SYNCENA is set, It's the time to wait after the posedge of the sync input before starting the 1st conversion of the sequence, or in case of a sequence without SYNCENA its the time between CONVERT goes high and the start of ADC conversion, basically it allows time for the first channel in the sequence to settle Current Time = (TCURR+1)x 250ns	4	rw	0x0

8.2.10.4 DATA1

0x50010D0C	DATA1	^

Data Out of CH1,.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0											

#	Field Name	Field Description	Width	Access	Reset
F0	DATA1	The result of ADC conversion of CH1	12	ro	0x0

8.2.10.5 DATA2

0x50010D10	DATA2	^

Data Out of CH2,.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0											

#	Field Name	Field Description	Width	Access	Reset
F0	DATA2	The result of ADC conversion of CH2	12	ro	0x0

8.2.10.6 DATA0345

0x50010D14	DATA0345	^

Data Out of CH0/CH3/CH4/CH5,.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0											

#	Field Name	Field Description	Width	Access	Reset
F0	DATA0345	The result of ADC conversion of CH0/CH3/CH4/CH5 depending on CHSEQ setting	12	ro	0x0

8.2.10.7 STATUS

0x50010D18	STATUS	^

Status Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F1						F0

#	Field Name	Field Description	Width	Access	Reset
F1	FSM	current state of the ADC Sequencer.	6	ro	0x0
F0	CONVDONE	The set Sequence of Conversions is Done. if set gets cleared with IRQCLR	1	ro	0x0

8.2.11 I/O Configuration & DFT pin control

IOCTRLA

Address	Register Name	Description
0x50011000	GPIO1	GPIO Pin 1 Control
0x50011004	GPIO2	GPIO Pin 2 Control
0x50011008	GPIO3	GPIO Pin 3 Control
0x5001100C	GPIO4	GPIO Pin 4 Control
0x50011010	GPIO5	GPIO Pin 5 Control
0x50011014	GPIO6	GPIO Pin 6 Control
0x50011018	LIN	LIN Pin Control
0x5001101C	LINSGFCONF	LINS Glitch Filter Configuration in active mode
0x50011020	LINMGFCONF	LINM Glitch Filter Configuration in active mode
0x50011024	LINTXDMONITOR	LIN TXD Dominant Timeout
0x50011028	LED	LED Pin Control
0x5001102C	ANALOGTESTMUXOVERRIDE	Analog Testmux Override
0x50011030	IRQ	IOCTRLA LINS/LINM TXD Dominant Monitor interrupts
0x50011034	LINSGFCONF1	LINS Glitch Filter Configuration in active mode
0x50011038	LINMGFCONF1	LINM Glitch Filter Configuration in active mode
0x5001103C	FILT_ACCESS	Glitch Filter access key

8.2.11.1 GPIO1

0x50011000	GPIO1	^

GPIO Pin 1 Control. GPIO Pin 1 has four seperate drivers: GPIO Controller, PWM Controller ,Testmux and LINM_RXD.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	F24							-	F16							-	-	-	-	-	-	-	-	F6		F5	F4	F3	F2	F0	

#	Field Name	Field Description	Width	Access	Reset
F24	MUXSEL	Selects debug signal to be output on gpio1. 0x0: PMUA (Power Management Unit Asic) QACK 0x1: PMUA (Power Management Unit Asic) Wakeup signal 0x2: PMUA (Power Management Unit Asic) snowflake 0x3: LIN Slave Output of 1st Stage Glitch Filter 0x4: LIN Slave Output of 2nd Stage Glitch Filter 0x5: LIN Slave Input of 1st Stage Glitch Filter Rxd 0x4: LIN Slave PHY Input Txd 0x7: LIN Master Output of 1st Stage Glitch Filter 0x8: LIN Master Output of 2nd Stage Glitch Filter 0x9: LIN Master Input of 1st Stage Glitch Filter Rxd 0xa: LIN Master Input PHY Txd 0x13: CRGA (Clock Reset Generation Asic) (scan_test_mode | pmu_CPclk4M) 0x14: CRGA (Clock Reset Generation Asic) (scan_test_mode | lf_rc_clk) 0x15: CRGA (Clock Reset Generation Asic) (scan_test_mode | hf_rc_clk) 0x16: CRGA (Clock Reset Generation Asic) (scan_test_mode | lf_rc_sts) 0x17: CRGA (Clock Reset Generation Asic)	7	rw	0x0

		(scan_test_mode | hf_rc_sts) 0x18: CRGA (Clock Reset Generation Asic) (scan_test_mode | clk_sys_gated) 0x19: CRGA (Clock Reset Generation Asic) (a_por_n) 0x1a: CRGA (Clock Reset Generation Asic) (bor_3v3_n) 0x1b: CRGA (Clock Reset Generation Asic) (ovtemp_flag) 0x1c: CRGA (Clock Reset Generation Asic) (bor_1v5_n) 0x1d: CRGA (Clock Reset Generation Asic) (wdt_bark) 0x2d: ADC ctrl (Analog to Digital Converter Controller) sync_rcvd[0] 0x2e: LIN Slave Input of Core rxd 0x2f: LIN Slave Output of Core txd 0x30: BOR CONTROL STATE MACHINE state[0] 0x31: BOR CONTROL STATE MACHINE state[1] 0x32: BOR CONTROL STATE MACHINE bor_bias_ena 0x33: BOR CONTROL STATE MACHINE bor_bias_ena_l 0x34: BOR CONTROL STATE MACHINE pmua_bor_bias_ena 0x35: BOR CONTROL STATE MACHINE hf_clk_allowed 0x36: BOR CONTROL STATE MACHINE hf_active 0x37: BOR CONTROL STATE MACHINE pmua_bor_arm_sync 0x38: BATTERY VOLTAGE MONITOR vbat_low 0x39: BATTERY VOLTAGE MONITOR vbat_high 0x3a: BATTERY VOLTAGE MONITOR vbat_low_flag 0x3b: BATTERY VOLTAGE MONITOR vbat_high_flag 0x3c: BATTERY VOLTAGE MONITOR vbat_low_dbnc 0x3d: BATTERY VOLTAGE MONITOR vbat_high_dbnc			

		0x3e: LIN Master Input of Core rxd 0x3f: LIN Master Output of Core txd			
F16	GPIO2_MUXSEL	Selects debug signal to be output on gpio2. Refer to GPIO1_MUX_SEL for signal selection	7	rw	0x0
F6	PWM_SEL	PWM output selection for PWM hardware mode. 0x0: PWM Channel0 selected in PWM hardware mode. 0x1: PWM Channel1 selected in PWM hardware mode. 0x2: PWM Channel2 selected in PWM hardware mode. 0x3: Reserved.	2	rw	0x0
F5	RDENA	read enable. 0x0: Disable Read path on the GPIO 0x1: Enable Read path on the GPIO	1	rw	0x0
F4	PDENA	pulldown enable. 0x0: Disable 100K Ohm Pull Down 0x1: Enable 100K Ohm Pull Down	1	rw	0x0
F3	PUENA	pullup enable (active-low). 0x0: Enable 100K Ohm Pull Up 0x1: Disable 100K Ohm Pull Up	1	rw	0x1
F2	LINM_SEL	LINM Connection Select.	1	rw	0x0
F0	HWMODE	hardware mode. 0x0: GPIO Mode. 'GPIO Barium' reads and writes data to the GPIO. Output Enable is controlled by GPIO Barium via the direction bit. Read Enable, Pull-Up, and Pull-Down are controlled by GPIO register in IOCTRLA. 0x1: PWM Mode. 'PWM Barium' writes data to the GPIO. 0x2: Testmux Mode. 'Digital Testmux' writes data to the GPIO. DEBUG Access must be enabled in the system control block to allow testmux outputs. 0x3: GPIO1_LINM_SEL=0 : LINM RXD;	2	rw	0x0

		GPIO1_LINM_SEL=1 : Single wire mode, LINM RXD/LINM TXD, Open-drain output.			

8.2.11.2 GPIO2

0x50011004 GPIO2 ^

GPIO Pin 2 Control. GPIO Pin 2 has four seperate drivers: GPIO Controller, PWM Controller ,Testmux and LINM_TXD.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F6		F5	F4	F3	F2	F0	

#	Field Name	Field Description	Width	Access	Reset
F6	PWM_SEL	PWM output selection for PWM hardware mode. 0x0: PWM Channel0 selected in PWM hardware mode. 0x1: PWM Channel1 selected in PWM hardware mode. 0x2: PWM Channel2 selected in PWM hardware mode. 0x3: Reserved.	2	rw	0x0
F5	RDENA	read enable. 0x0: Disable Read path on the GPIO 0x1: Enable Read path on the GPIO	1	rw	0x0
F4	PDENA	pulldown enable. 0x0: Disable 100K Ohm Pull Down 0x1: Enable 100K Ohm Pull Down	1	rw	0x0
F3	PUENA	pullup enable (active-low). 0x0: Enable 100K Ohm Pull Up 0x1: Disable 100K Ohm Pull Up	1	rw	0x1
F2	GPIO2_HW_MODE_MSB	MSB of GPIO2_HW_MODE. 0x0: GPIO Mode. 'GPIO Barium' reads and writes data to the GPIO. Output Enable is	1	rw	0x0

		controlled by GPIO Barium via the direction bit. Read Enable, Pull-Up, and Pull-Down are controlled by GPIO register in IOCTRLA. 0x1: Testmux Mode. 'Digital Testmux' writes data to the GPIO. DEBUG Access must be enabled in the system control block to allow testmux outputs.			
F0	HWMODE	hardware mode. 0x0: GPIO Mode. 'GPIO Barium' reads and writes data to the GPIO. Output Enable is controlled by GPIO Barium via the direction bit. Read Enable, Pull-Up, and Pull-Down are controlled by GPIO register in IOCTRLA. 0x1: PWM Mode. 'PWM Barium' writes data to the GPIO. 0x2: LINS PHY TXD Drive Mode. GPIO input connects to LINS PHY TXD. DEBUG Access must be enabled in the system control block to drive LINS PHY TXD outputs. 0x3: LINM Core TXD Monitor.	2	rw	0x0

8.2.11.3 GPIO3

0x50011008 **GPIO3** ^

GPIO Pin 3 Control. GPIO Pin 3 has four seperate drivers: GPIO Controller, PWM Controller , Testmux and LINS_RXD.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F8	F6		F5	F4	F3	F2	F0	

#	Field Name	Field Description	Width	Access	Reset
F8	GPIO3_HW_MODE_MSB	MSB of GPIO3_HW_MODE. 0x4: Monitor LINS Input of 1st Stage Glitch	1	rw	0x0

		Filter Rxd. 0x5: Monitor LINM Input of 1st Stage Glitch Filter Rxd. 0x6: Monitor 1st Stage output of LINS RX Glitch filter. 0x7: Monitor 1st Stage output of LINM RX Glitch filter.			
F6	PWM_SEL	PWM output selection for PWM hardware mode. 0x0: PWM Channel0 selected in PWM hardware mode. 0x1: PWM Channel1 selected in PWM hardware mode. 0x2: PWM Channel2 selected in PWM hardware mode. 0x3: Reserved.	2	rw	0x0
F5	RDENA	read enable. 0x0: Disable Read path on the GPIO 0x1: Enable Read path on the GPIO	1	rw	0x0
F4	PDENA	pulldown enable. 0x0: Disable 100K Ohm Pull Down 0x1: Enable 100K Ohm Pull Down	1	rw	0x0
F3	PUENA	pullup enable (active-low). 0x0: Enable 100K Ohm Pull Up 0x1: Disable 100K Ohm Pull Up	1	rw	0x1
F2	LINS_SEL	LINS Connection Select.	1	rw	0x0
F0	HWMODE	2-LSB of GPIO3 hardware mode. 0x0: GPIO Mode. 'GPIO Barium' reads and writes data to the GPIO. Output Enable is controlled by GPIO Barium via the direction bit. Read Enable, Pull-Up, and Pull-Down are controlled by GPIO register in IOCTRLA. 0x1: PWM Mode. 'PWM Barium' writes data to the GPIO. 0x2: Testmux Mode. LINM RXD connects to GPIO output. DEBUG Access must be enabled in the system control block to allow testmux outputs.	2	rw	0x0

		0x3: LINS_SEL=0 : LINS RXD; LINS_SEL=1 : Single wire mode, LINS RXD/LINS TXD, Open-drain output.			

8.2.11.4 GPIO4

0x5001100C GPIO4 ^

GPIO Pin 4 Control. GPIO Pin 4 has four seperate drivers: GPIO Controller, PWM Controller ,Testmux and LINS_TXD.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F6	F5	F4	F3	F2	F0	

#	Field Name	Field Description	Width	Access	Reset
F6	PWM_SEL	PWM output selection for PWM hardware mode. 0x0: PWM Channel0 selected in PWM hardware mode. 0x1: PWM Channel1 selected in PWM hardware mode. 0x2: PWM Channel2 selected in PWM hardware mode. 0x3: Reserved.	2	rw	0x0
F5	RDENA	read enable. 0x0: Disable Read path on the GPIO 0x1: Enable Read path on the GPIO	1	rw	0x0
F4	PDENA	pulldown enable. 0x0: Disable 100K Ohm Pull Down 0x1: Enable 100K Ohm Pull Down	1	rw	0x0
F3	PUENA	pullup enable (active-low). 0x0: Enable 100K Ohm Pull Up 0x1: Disable 100K Ohm Pull Up	1	rw	0x1

F2	GPIO4_HW_MODE_MSB	MSB of GPIO4_HW_MODE. 0x4: Monitor LINS Core Rxd input. 0x5: Monitor LINM Core Rxd input. 0x6: Monitor 2nd Stage output of LINS RX Glitch filter. 0x7: Monitor 2nd Stage output of LINM RX Glitch filter.	1	rw	0x0
F0	HWMODE	2-LSB of GPIO4 hardware mode. 0x0: GPIO Mode. 'GPIO Barium' reads and writes data to the GPIO. Output Enable is controlled by GPIO Barium via the direction bit. Read Enable, Pull-Up, and Pull-Down are controlled by GPIO register in IOCTRLA. 0x1: PWM Mode. 'PWM Barium' writes data to the GPIO. 0x2: Testmux Mode. GPIO input connects to LINM TXD. 0x3: LINS CORE TXD Monitor	2	rw	0x0

8.2.11.5 GPIO5

0x50011010 **GPIO5** ^

GPIO Pin 5 Control. GPIO Pin 5 has four seperate drivers: GPIO Controller, PWM Controller , Testmux and LINS_RXD.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F8	F6		F5	F4	F3	F2	F0	

#	Field Name	Field Description	Width	Access	Reset
F8	GPIO5_HW_MODE_MSB	MSB of GPIO5_HW_MODE. 0x4: Monitor LINS Input of 1st Stage Glitch Filter Rxd. 0x5: Monitor LINM Input of 1st Stage Glitch Filter Rxd.	1	rw	0x0

		0x6: Monitor 1st Stage output of LINS RX Glitch filter. 0x7: Monitor 1st Stage output of LINM RX Glitch filter.			
F6	PWM_SEL	PWM output selection for PWM hardware mode. 0x0: PWM Channel0 selected in PWM hardware mode. 0x1: PWM Channel1 selected in PWM hardware mode. 0x2: PWM Channel2 selected in PWM hardware mode. 0x3: Reserved.	2	rw	0x0
F5	RDENA	read enable. 0x0: Disable Read path on the GPIO 0x1: Enable Read path on the GPIO	1	rw	0x0
F4	PDENA	pulldown enable. 0x0: Disable 100K Ohm Pull Down 0x1: Enable 100K Ohm Pull Down	1	rw	0x0
F3	PUENA	pullup enable (active-low). 0x0: Enable 100K Ohm Pull Up 0x1: Disable 100K Ohm Pull Up	1	rw	0x1
F2	LINS_SEL	LINS Connection Select. 0x0: LINS RXD External input Mode. 0x1: Single wire mode, LINS RXD/LINS TXD, Open-drain output.	1	rw	0x0
F0	GPIO5HWMODE	hardware mode. 0x0: GPIO Mode. 'GPIO Barium' reads and writes data to the GPIO. Output Enable is controlled by GPIO Barium via the direction bit. Read Enable, Pull-Up, and Pull-Down are controlled by GPIO register in IOCTRLA. 0x1: PWM Mode. 'PWM Barium' writes data to the GPIO. 0x2: Testmux Mode. LINM RXD connects to GPIO output. DEBUG Access must be enabled in the system control block to allow testmux outputs.	2	rw	0x0

		0x3: LINS_SEL=0 : LINS RXD; LINS_SEL=1 : Single wire mode, LINS RXD/LINS TXD, Open-drain output; LINS_SEL=2 : Testmux Mode, 1st Stage output of LINS RX Glitch filter.			

8.2.11.6 GPIO6

0x50011014 GPIO6 ^

GPIO Pin 6 Control. GPIO Pin 6 has four seperate drivers: GPIO Controller, PWM Controller ,Testmux and LINS_TXD.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F6	F5	F4	F3	F2	F0	

#	Field Name	Field Description	Width	Access	Reset
F6	PWM_SEL	PWM output selection for PWM hardware mode. 0x0: PWM Channel0 selected in PWM hardware mode. 0x1: PWM Channel1 selected in PWM hardware mode. 0x2: PWM Channel2 selected in PWM hardware mode. 0x3: Reserved.	2	rw	0x0
F5	RDENA	read enable. 0x0: Disable Read path on the GPIO 0x1: Enable Read path on the GPIO	1	rw	0x0
F4	PDENA	pulldown enable. 0x0: Disable 100K Ohm Pull Down 0x1: Enable 100K Ohm Pull Down	1	rw	0x0

F3	PUENA	pullup enable (active-low). 0x0: Enable 100K Ohm Pull Up 0x1: Disable 100K Ohm Pull Up	1	rw	0x1
F2	GPIO6_HW_MODE_MSB	MSB of GPIO6_HW_MODE. 0x4: Monitor LINS Core Rxd input. 0x5: Monitor LINM Core Rxd input. 0x6: Monitor 2nd Stage output of LINS RX Glitch filter. 0x7: Monitor 2nd Stage output of LINM RX Glitch filter.	1	rw	0x0
F0	HWMODE	2-LSB of GPIO6 hardware mode. 0x0: GPIO Mode. 'GPIO Barium' reads and writes data to the GPIO. Output Enable is controlled by GPIO Barium via the direction bit. Read Enable, Pull-Up, and Pull-Down are controlled by GPIO register in IOCTRLA. 0x1: PWM Mode. 'PWM Barium' writes data to the GPIO. 0x2: Testmux Mode. GPIO input connects to LINM TXD. 0x3: LINS CORE TXD Monitor	2	rw	0x0

8.2.11.7 LIN

0x50011018 **LIN** ^

LIN Pin Control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	-	-	-	F24	-	-	-	-	F19	F18	F17	F16	-	F14	F13	F12	F11	-	-	F8	-	F6	F5	-	F3	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F31	PMODE	LIN Power Mode. Control LINS/LINM power state in hibernate mode. 0x0: Regardless of the related enable bits, LIN TX analog parts will be shut-down in hibernate mode, unless any LIN dominant signal is detected.	1	rw	0x0

		0x1: LIN TX analog parts are still controlled by theirs corresponding enable bits.			
F24	SWON_LOCK	SWON Lock Bit.	1	rw	0x0
F19	LINM_PUOFF_TIMEOUT	LINM 1K Pullup disable in dominant TimeOut condition. Set to disable LINM 1K pullup in case that lin bus is shorted to ground(Bus idle dominant timeout is detected) for saving power. LINS 1K Pullup will be recovered automatically if bus idle dominant timeout is released by any bus activity. If this bit is set & SWON = 1, LINM's 30K pullup will be enabled for preventing bus floating. Only reset by power-on sequence.	1	rw	0x1
F18	LINS_PUOFF_TIMEOUT	LINS Pullup Disable in dominant TimeOut condition. Set to disable LINS 30K pullup in case that lin bus is shorted to ground(Bus idle dominant timeout is detected) for saving power. LINS Pullup will be recovered automatically if bus idle dominant timeout is released by any bus activity. Only reset by power-on sequence.	1	rw	0x1
F17	SWOFF_TIMEOUT	Switch off in dominant TimeOut condition. Set to disconnect lin switch in case that lin bus is shorted to ground(Bus idle dominant timeout is detected) for saving power. LIN Switch will be recovered automatically if bus idle dominant timeout is released by any bus activity. Only reset by power-on sequence.	1	rw	0x1
F16	SWON	LIN Dual Mode Switch On. Set to enable dual-mode lin switch. Only reset by power-on sequence. This bit can be locked by setting SWON_LOCK.	1	rw	0x1
F14	LINM_RXENA	LIN receive enable.	1	rw	0x0
F13	LINM_TXENA	LIN transmit enable.	1	rw	0x0
F12	LINM_PU1K_ENA	LIN 1K pullup enable.	1	rw	0x1
F11	LINM_PU30K_ENA	LIN 30K pullup enable.	1	rw	0x0
F8	LINM_HWMODE	LIN Master hardware mode. 0x0: Hardware Mode Disabled. GPIO4 writes/reads the LIN I/O pin. 0x1: Hardware Mode Enabled. LIN peripheral writes/read the LIN I/O pin.	1	rw	0x0
F6	LINS_RXENA	LIN receive enable.	1	rw	0x0

F5	LINS_TXENA	LIN transmit enable.	1	rw	0x0
F3	LINS_PU30K_ENA	LIN 30K pullup enable.	1	rw	0x1
F0	LINS_HWMODE	LIN Slave hardware mode. 0x0: Hardware Mode Disabled. GPIO3 writes/reads the LIN I/O pin. 0x1: Hardware Mode Enabled. LIN peripheral writes/read the LIN I/O pin.	1	rw	0x0

8.2.11.8 LINSGFCONF

0x5001101C	LINSGFCONF	^

LINS Glitch Filter Configuration in active mode.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	F16							-	F8							-	-	-	-	-	-	F0	

#	Field Name	Field Description	Width	Access	Reset
F16	LINSDBNCTHRES1	LINS Debounce Threshold for 0 to 1.	7	rw	0x28
F8	LINSDBNCTHRES0	LINS Debounce Threshold for 1 to 0.	7	rw	0x28
F3	LINS_RX_GF_ENA_2ND	LINS RXD 2nd Glitch Filter enables. Enable LINS Glitch Filter 2nd stage.	1	rw	0x01
F2	LINS_RX_GF_ENA_1ST	LINS RXD 1st Glitch Filter enables. Enable LINS Glitch Filter 1st stage.	1	rw	0x01
F0	LINSRXGFENA	LINS RXD Glitch Filter enables.	2	rw	0x3

8.2.11.9 LINMGFCONF

0x50011020	LINMGFCONF	^

LINM Glitch Filter Configuration in active mode.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	F16							-	F8							-	-	-	-	-	-	F0	

#	Field Name	Field Description	Width	Access	Reset
F16	LINMDBNCTHRES1	LINM Debounce Threshold for 0 to 1.	7	rw	0x28
F8	LINMDBNCTHRES0	LINM Debounce Threshold for 1 to 0.	7	rw	0x28
F3	LINM_RX_GF_ENA_2ND	LINM RXD 2nd Glitch Filter enables. Enable LINS Glitch Filter 2nd stage.	1	rw	0x01
F2	LINM_RX_GF_ENA_1ST	LINM RXD 1st Glitch Filter enables. Enable LINS Glitch Filter 1st stage.	1	rw	0x01
F0	LINMRXGFENA	LINM RXD Glitch Filter enables.	2	rw	0x3

8.2.11.10 LINTXMONITOR

0x50011024	LINTXDMONITOR	^

LIN TXD Dominant Timeout.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F9	F8	-	-	-	-	-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F9	LINMTXDTIMEOUTDOMINANT	Tx Dominant Timeout. The bit is set by LINM TxD monitor if LINM's TxD is stuck at dominant output for 64ms. A dominant to recessive transition of the TxD will clear this bit. LIN's TX will be disabled automatically when this bit is set.	1	ro	0x0

F8	LINSTXDTIMEOUTDOMINANT	Tx Dominant Timeout. The bit is set by LINS TxD monitor if LINS's TxD is stuck at dominant output for 64ms. A dominant to recessive transition of the TxD will clear this bit. LIN's TX will be disabled automatically when this bit is set.	1	ro	0x0
F1	LINMTXDMONITORENA	LINM TxD Monitor enable.	1	rw	0x1
F0	LINSTXDMONITORENA	LINS TxD Monitor enable.	1	rw	0x1

8.2.11.11 LED

0x50011028 LED ^

LED Pin Control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F16	F15	-	F9					F8	-	F4			-	F0		

#	Field Name	Field Description	Width	Access	Reset
F16	GAIN_SEL	LED Sense AFE gain select. vbat-vled=GAIN*V_ADC, where V_ADC is voltage measured by ADC channle2, and GAIN is selected by GAIN_SEL as following: 0x0: GAIN=4 0x1: GAIN=8	1	rw	0x0
F15	VFW_ENA	LED Forward Voltage Current Enable. Set to enable the independent LED VFW current source(maximum=5mA). When ADC CH2 measurement is active, the LED channel selected by CH2_SEL will be driven by LED_VFW current source.	1	rw	0x0
F9	SENSE_CTRL	LED. LED Sense Control bits for override control/debug.	5	rw	0x0
F8	SENSE_ENA	LED Forward Voltage Sense Enable. Set to enable LED forward voltage sense module. After setting this bit, it's recommended to wait ~40us before ADC conversion for LED_SENSE to settle down.	1	rw	0x1

F4	DATA	LED Data Out. When the LED hardware mode is disabled, then the data in this register bit is used to drive the LED driver. Each bit controls the corresonding LED Channel respectively.	3	rw	0x0
F0	HWMODE	LED hardware mode. LED Hardware Mode Enable. Each bit controls the corresponding LED Channel respectively. 0x0: Hardware Mode Disabled. LED_DATA register drives the LED Data Output pin. Read is not available on this pin. 0x1: Hardware Mode Enabled. PWM_BARIUM peripheral drives the LED Data Output pin. Read is not available on this pin.	3	rw	0x0

8.2.11.12 ANALOGTESTMUXOVERRIDE

0x5001102C ANALOGTESTMUXOVERRIDE ^

Analog Testmux Override. This register controls the multiplexers for analog signals.
The select bit allows firmware to control the corresponding select field (in other words, firmware control).
The following table is intended to be a helpful guide in what data should be written to this register in order to connect a source and target together.
Note- Care should be taken to write zero to this register between connection changes. This ensures a clean break between selections.

Data to write at address 0x50011018 to enable connection

Source Description	Target Description	Data to write to connect Source to Target
3.3V Digital Supply	GPIO1	0x0101_0006
3.3V Analog Supply	GPIO1	0x0102_0006
1.5V MCU Supply	GPIO1	0x0104_0006
Band Gap- vbg_buffered raw	GPIO1	0x0108_0006

VDD Limit = Measured Voltage * 4	GPIO2	0x0210_0006
VDD Protected = Measured Voltage * 9	GPIO2	0x0220_0006
Temperature Sensor	GPIO2	0x0240_0006
Aux Bandgap supply	GPIO2	0x0280_0006
Band Gap	ADC	0x0000_0101
Accurate VBAT	ADC	0x0000_0201
LED Forward Voltage	ADC	0x0000_0401
Temperature Sensor or accurate_vbat	ADC	0x0000_0801
GPIO1/2/3/4/5/6	ADC	0x0000_1001
VDD1.5V	ADC	0x0000_2001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	F24						-	F16							-	-	F8						-	-	-	-	-	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F24	ADCSELREG	Firmware Debug Value. need to be configured TOGETHER WITH gpio_con_reg to enable gpio1/2/3/4/5/6 PAD output. (ADC_SEL_SEL also need to be set to 1) 0x1: Enable GPIO1 analog connection 0x2: Enable GPIO2 analog connection 0x4: Enable GPIO3 analog connection 0x8: Enable GPIO4 analog connection 0x10: Enable GPIO5 analog connection 0x20: Enable GPIO6 analog connection	6	rw	0x0
F16	GPIOCONREG	Firmware Debug Value. GPIO1/2 test MUX select 0x1: Select 3.3V digital supply to GPIO1 0x2: Select 3.3v analog supply to GPIO1	7	rw	0x0

		0x4: Select 1.5v MCU supply to GPIO1 0x8: Select Bandgap supply to GPIO1 0x10: Select vdd_lim to GPIO2 0x20: Select vdd_prt to GPIO2 0x40: Select tempsensor to GPIO2			
F8	ADCCONREG	Firmware Debug Value. Contains the output value when the ADC_CON_SEL firmware select bit is set. 0x1: Select ADC_VCM(adc voltage reference) to ADC (Need to enable ADC bias first) 0x2: Select Accurate VBAT to ADC 0x4: Select LED0/1/2(when when adc.cntrl.ch2sel=0/1/2) Forward Voltage to ADC 0x8: Select Tempsensor to ADC 0x10: Select GPIO1~6(Determined by adc.cntrl.ch4sel) to ADC 0x20: Select VDD1.5v to ADC	6	rw	0x0
F2	ADCSELSEL	Hardware/Firmware Select. 0x0: Hardware Controlled. 0x1: ADC_SEL_REG controls output.	1	rw	0x0
F1	GPIOCONSEL	Hardware/Firmware Select. 0x0: Hardware Controlled. 0x1: GPIO_CON_REG controls output.	1	rw	0x0
F0	ADCCONSEL	Hardware/Firmware Select. 0x0: Hardware Controlled. 0x1: ADC_CON_REG controls output.	1	rw	0x0

8.2.11.13 IRQ

0x50011030	IRQ	^

IOCTRLA LINS/LINM TXD Dominant Monitor interrupts. Contains the the enable, clear, status and active flag for the LINS/LINM TXD Dominant Monitor interrupt sources.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	F25	F24	-	-	-	-	-	-	F17	F16	-	-	-	-	-	-	F9	F8	-	-	-	-	-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F25	LINM_TXD_DOM	LINM TXD Dominant Monitor interrupt active.	1	ro	0x0
F24	LINS_TXD_DOM	LINS TXD Dominant Monitor interrupt active.	1	ro	0x0
F17	LINM_TXD_DOM	LINM TXD Dominant Monitor interrupt status.	1	ro	0x0
F16	LINS_TXD_DOM	LINS TXD Dominant Monitor interrupt status.	1	ro	0x0
F9	LINM_TXD_DOM	LINM TXD Dominant Monitor interrupt clear. Autoclear: inlcudes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F8	LINS_TXD_DOM	LINS TXD Dominant Monitor interrupt clear. Autoclear: inlcudes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F1	LINM_TXD_DOM	LINM TXD Dominant Monitor interrupt enable.	1	rw	0x0
F0	LINS_TXD_DOM	LINS TXD Dominant Monitor interrupt enable.	1	rw	0x0

8.2.11.14 LINSGFCONF1

0x50011034 LINSGFCONF1 ^

LINS Glitch Filter Configuration in active mode..

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	F24							-	F16							-	F8							-	F0						

#	Field Name	Field Description	Width	Access	Reset
F24	LINS_DBNC_THRES1_2ND	2nd Stage LINS Debounce Threshold for 0 to 1. 2nd Stage LINS Debounce Threshold for 0 to 1, detect '1' width of (T_clksys*resetvalue = 62.5ns*32 = 2[us]).	7	rw	0x20

F16	LINS_DBNC_THRES0_2ND	2nd Stage LINS Debounce Threshold for 1 to 0. 2nd Stage LINS Debounce Threshold for 1 to 0, detect '0' width of (T_clksys*resetvalue = 62.5ns*16 = 1[us]).	7	rw	0x10
F8	LINS_DBNC_THRES1_1ST	1st Stage LINS Debounce Threshold for 0 to 1. 1st Stage LINS Debounce Threshold for 0 to 1, detect '1' width of (T_clksys*resetvalue = 62.5ns*0 = 0[us]).	7	rw	0x0
F0	LINS_DBNC_THRES0_1ST	1st Stage LINS Debounce Threshold for 1 to 0. 1st Stage LINS Debounce Threshold for 1 to 0, detect '0' width of (T_clksys*resetvalue = 62.5ns*8 = 0.5[us]).	7	rw	0x8

8.2.11.15 LINMGFCONF1

0x50011038 LINMGFCONF1 ^

LINM Glitch Filter Configuration in active mode..

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	F24							-	F16							-	F8							-	F0						

#	Field Name	Field Description	Width	Access	Reset
F24	LINM_DBNC_THRES1_2ND	2nd Stage LINM Debounce Threshold for 0 to 1. 2nd Stage LINM Debounce Threshold for 0 to 1, detect '1' width of (T_clksys*resetvalue = 62.5ns*32 = 2[us]).	7	rw	0x20
F16	LINM_DBNC_THRES0_2ND	2nd Stage LINM Debounce Threshold for 1 to 0. 2nd Stage LINM Debounce Threshold for 1 to 0, detect '0' width of (T_clksys*resetvalue = 62.5ns*16 = 1[us]).	7	rw	0x10
F8	LINM_DBNC_THRES1_1ST	1st Stage LINM Debounce Threshold for 0 to 1. 1st Stage LINM Debounce Threshold for 0 to 1, detect '1' width of (T_clksys*resetvalue = 62.5ns*0 = 0[us]).	7	rw	0x0
F0	LINM_DBNC_THRES0_1ST	1st Stage LINM Debounce Threshold for 1 to 0. 1st Stage LINM Debounce Threshold for 1 to 0, detect '0' width of (T_clksys*resetvalue = 62.5ns*8 = 0.5[us]).	7	rw	0x8

8.2.11.16 FILT_ACCESS

0x5001103C FILT_ACCESS ^

Glitch Filter access key.																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F31	FILT_UNLOCK	Set Only bit. Write 1 to this bit to un-lock FILT_CODE bits.	1	rw	0x0

8.2.12 System configuration and retention memory

SYSCTRLA		
Address	**Register Name**	**Description**
0x50012000	RETAIN0	Retained data 0
0x50012004	RETAIN1	Retained data 1
0x50012008	DEBUG_ACCESS_KEY	Debug access key
0x5001200C	DEBUG_ACCESS_ENABLED	Debug access enabled
0x50012010	TRIM_ACCESS_KEY	Trim access key
0x50012014	TRIM_ACCESS_ENABLED	Trim access enabled
0x50012018	PMU_TRIM	PMU trim values
0x5001201C	LF_OSC_TRIM	Trim controls for the low frequency (32k/250KHz) oscillators
0x50012020	HF_OSC_TRIM	Trim controls for the high frequency (16MHz) oscillator

0x50012024	BIAS	Bias Control
0x50012028	TRIMLED0	High Voltage LED trim
0x5001202C	TRIMLED1	High Voltage LED trim
0x50012030	TRIMLED2	High Voltage LED trim
0x50012034	TRIMVFW	VFW Current Trim
0x50012038	LIN	LIN IO Control (Trim access need to be enabled before Written)
0x5001203C	DFTCODE	DFT Unlock Code
0x50012040	DFT_ACCESS_ENABLED	DFT access enabled
0x50012044	DFTTESTMODESTART	DFT Mode Start
0x50012048	NAME	ASIC name
0x5001204C	REV	Silicon Revision
0x50012050	BORTESTMODE	BOR Testmode Enable

8.2.12.1 RETAIN0

0x50012000	RETAIN0	^

Retained data 0.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0			

#	Field Name	Field Description	Width	Access	Reset

F0	RETAIN0	Firmware scratch register 0. Only reset at power-on (e.g contents retained in Hibernate mode and retained despite any hard or soft resets).	4	rw	0x0

8.2.12.2 RETAIN1

0x50012004 RETAIN1 ^

Retained data 1.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0			

#	Field Name	Field Description	Width	Access	Reset
F0	RETAIN1	Firmware scratch register 1 (0x1). Contents retained in Hibernate mode - but lost after any hard or soft reset.	4	rw	0x0

8.2.12.3 DEBUG_ACCESS_KEY

0x50012008 DEBUG_ACCESS_KEY ^

Debug access key.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0			

#	Field Name	Field Description	Width	Access	Reset
F31	DEBUG_LOCK	Set Only bit. Set this bit to lock DEBUG_CODE bits.	1	rw	0x0
F0	DEBUG_ACCESS_KEY	Write the value 0x5 to this register to enable debug options. Write any other value to disable the debug options.	4	rw	0x0

8.2.12.4 DEBUG_ACCESS_ENABLED

0x5001200C	DEBUG_ACCESS_ENABLED	^

Debug access enabled.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	DEBUG_ACCESS_ENABLED	A status flag that is set when debug access is enabled	1	ro	0x0

8.2.12.5 TRIM_ACCESS_KEY

0x50012010	TRIM_ACCESS_KEY	^

Trim access key.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0			

#	Field Name	Field Description	Width	Access	Reset
F31	TRIM_LOCK	Set Only bit. Write 1 to this bit to lock TRIM_CODE bits.	1	rw	0x0
F0	TRIM_ACCESS_KEY	Write the value 0xe to this register to enable 'trim access' (which allows write access to various trim settings and production test options). Write any other value to disable trim access.	4	rw	0x0

8.2.12.6 TRIM_ACCESS_ENABLED

0x50012014	TRIM_ACCESS_ENABLED	^

Trim access enabled.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	TRIM_ACCESS_ENABLED	A status flag that is set when trim access is enabled	1	ro	0x0

8.2.12.7 PMU_TRIM

0x50012018	PMU_TRIM	^

PMU trim values.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F8						-	F4			-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F8	RESISTOR_TRIM	V2I Resistor Trim. Selects the resistor trim value for the V2I circuit. The larger RESISTOR_TRIM value, the lower V2I current.	6	rw	0x1E
F4	TRIM	Band Gap Trim. Selects the trim value for the band gap reference circuit. The larger TRIM value, the higher bandgap voltage.	3	rw	0x4

8.2.12.8 LF_OSC_TRIM

0x5001201C	LF_OSC_TRIM	^

Trim controls for the low frequency (32k/250KHz) oscillators.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	TRIM_LF_RC	LF RC oscillator trim. The following values are only used as a reference: 0x0: freq(32k)=19.06kHz , frea(250k)=131.1Khz 0xaf: freq(32k)=38.57kHz , frea(250k)=255.9Khz 0xff: freq(32k)=66.06kHz , frea(250k)=421.7Khz	8	rw	0xAF

8.2.12.9 HF_OSC_TRIM

0x50012020	HF_OSC_TRIM	^

Trim controls for the high frequency (16MHz) oscillator.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	F16								-	-	-	-	F9			F8	F0							

#	Field Name	Field Description	Width	Access	Reset
F16	SSCDIV	SSC Clock Divider. SSC Freq = SYS_FREQ/[(SSC_DIV+1) *(SSC_DEEP+1) *4].	8	rw	0x28
F9	SSCDEEP	SSC Depth Configuration.	3	rw	0x0
F8	SSCENA	SSC Enable.	1	rw	0x0
F0	TRIM_HF_RC	High Frequency RC Oscillator trim. TRIM bits will be changed if SSC is enabled. Reload the trim bits from Flash if SSC is disabled while the change has happened. Following value only used as a reference: 0xa: freq=26.08Mhz	8	rw	0x34

		0x80: freq=9.62Mhz 0xfa: freq=5.94Mhz			

8.2.12.10 BIAS

0x50012024 BIAS ^

Bias Control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F1	LEDBIASREG	High Voltage LED bias select register. If LED_BIAS_SEL is set, then LED_BIAS_REG allows override access to the LED BIAS signal.	1	rw	0x0
F0	LEDBIASSEL	High Voltage LED bias select. 0x0: The LED Bias is enabled and disabled by the pmu hardware state machine by default. 0x1: The value of the LED_BIAS_REG field is what is used to drive the LED_BIAS signal. (override mode)	1	rw	0x0

8.2.12.11 TRIMLED0

0x50012028 TRIMLED0 ^

High Voltage LED trim.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F16									-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset

F16	TRIM0	LED trim (120uA step).	9	rw	0xFA

8.2.12.12 TRIMLED1

0x5001202C **TRIMLED1** ^

High Voltage LED trim.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F16									-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F16	TRIM1	LED trim (120uA step).	9	rw	0xFA

8.2.12.13 TRIMLED2

0x50012030 **TRIMLED2** ^

High Voltage LED trim.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	F16									-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

#	Field Name	Field Description	Width	Access	Reset
F16	TRIM2	LED trim (120uA step).	9	rw	0xFA

8.2.12.14 TRIMVFW

0x50012034	TRIMVFW	^

VFW Current Trim.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	TRIMVFW	PN Forward Voltage Current trim (10uA step).	8	rw	0xC8

8.2.12.15 LIN

0x50012038	LIN	^

LIN IO Control (Trim access need to be enabled before Written).

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F9	F8	F6		F4		F2		F0	

#	Field Name	Field Description	Width	Access	Reset
F9	TXLINMRISESLOPE	LIN Slave IO Rise Slope select.	1	rw	0x1
F8	TXLINSRISESLOPE	LIN Slave IO Rise Slope select.	1	rw	0x1
F6	LINMTX_BIAS_BOOST	LIN Master IO TX Bias select. Select LIN IO TX Pull Down Current. 0x0: ~61 mA 0x1: ~83 mA 0x2: ~105 mA 0x3: ~126 mA	2	rw	0x0
F4	LINSTX_BIAS_BOOST	LIN Slave IO TX Bias select. Select LIN IO TX Pull Down Current. 0x0: ~61 mA 0x1: ~83 mA	2	rw	0x0

		0x2: ~105 mA 0x3: ~126 mA			
F2	TXLINM_DR_SLOPE	LIN Master IO Drive Slope select. Slew from 40%*Vbat to 60%*Vbat @Vbat=13V,Cbus=1nF. 0x0: when TXLINM_RISE_SLOPE=0: slewRate_pos = 2.1V/us, slewRate_neg = 2.2V/us 0x1: when TXLINM_RISE_SLOPE=0: slewRate_pos = 4.0V/us, slewRate_neg = 4.3V/us 0x2: when TXLINM_RISE_SLOPE=0: slewRate_pos = 4.9V/us, slewRate_neg = 6.3V/us 0x3: when TXLINM_RISE_SLOPE=0: slewRate_pos = 5.1V/us, slewRate_neg = 30.3V/us 0x0: when TXLINM_RISE_SLOPE=1: slewRate_pos = 5.1V/us, slewRate_neg = 2.2V/us 0x1: when TXLINM_RISE_SLOPE=1: slewRate_pos = 5.1V/us, slewRate_neg = 4.3V/us 0x2: when TXLINM_RISE_SLOPE=1: slewRate_pos = 5.1V/us, slewRate_neg = 6.3V/us 0x3: when TXLINM_RISE_SLOPE=1: slewRate_pos = 5.1V/us, slewRate_neg = 30.3V/us	2	rw	0x2
F0	TXLINS_DR_SLOPE	LIN Slave IO Drive Slope select. Slew from 40%*Vbat to 60%*Vbat @Vbat=13V,Cbus=1nF. 0x0: when TXLINS_RISE_SLOPE=0: slewRate_pos = 2.1V/us, slewRate_neg = 2.2V/us 0x1: when TXLINS_RISE_SLOPE=0: slewRate_pos = 4.0V/us, slewRate_neg = 4.3V/us 0x2: when TXLINS_RISE_SLOPE=0: slewRate_pos = 4.9V/us, slewRate_neg = 6.3V/us 0x3: when TXLINS_RISE_SLOPE=0: slewRate_pos = 5.1V/us, slewRate_neg = 30.3V/us 0x0: when TXLINS_RISE_SLOPE=1: slewRate_pos = 5.1V/us, slewRate_neg = 2.2V/us 0x1: when TXLINS_RISE_SLOPE=1: slewRate_pos = 5.1V/us, slewRate_neg = 4.3V/us 0x2: when TXLINS_RISE_SLOPE=1: slewRate_pos = 5.1V/us, slewRate_neg = 6.3V/us 0x3: when TXLINS_RISE_SLOPE=1: slewRate_pos = 5.1V/us, slewRate_neg = 30.3V/us	2	rw	0x2

8.2.12.16 DFTCODE

0x5001203C	DFTCODE	^

DFT Unlock Code.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F31	DFT_LOCK	Set Only bit. Write 1 to this bit to lock DFT related config bits.	1	rw	0x0
F0	DFTCODE	Test Mode Unlock Enable Code. 0x1C needs to be written to this register to unlock the DFT_TESTMODE_SEL and DFT_TESTMODE_START registers.	8	wo	0x0

8.2.12.17 DFT_ACCESS_ENABLED

0x50012040 DFT_ACCESS_ENABLED ^

DFT access enabled.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	DFT_ACCESS_ENABLED	A status flag that is set when DFT access is enabled.	1	ro	0x0

8.2.12.18 DFTTESTMODESTART

0x50012044 DFTTESTMODESTART ^

DFT Mode Start.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	DFTTESTMODESTART	Puts the ASIC into DFT testmode. Once the start bit is set, the I/O configuration will switch from Application mode to DFT Test Mode. The General Purpose I/Os will be configured as a JTAG interface. Once Test Mode is enabled, the ASIC will be boundary terminated and the processor will lose the ability to communicate with any ASIC peripherals. A chip power cycle is required to get out of the DFT test mode. Test Mode Enable state.	1	wo	0x0

8.2.12.19 NAME

0x50012048 NAME ^

ASIC name.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	NAME	ASIC name. A read from this register will return the ASIC name	32	ro	N/A

8.2.12.20 REV

0x5001204C REV ^

Silicon Revision.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0															

#	Field Name	Field Description	Width	Access	Reset
F0	REV	Silicon Revision. A read from this register will return the ASCII silicon revision (e.g. ASCII C0 is 0x4330)	16	ro	N/A

8.2.12.21 BORTESTMODE

0x50012050	BORTESTMODE	^

BOR Testmode Enable.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	ENABORTESTMODE	BOR Testmode Enable. 0x0: BOR Testmode Disabled: Reference Voltage for BOR is from Band Gap (Functional Mode) 0x1: BOR Testmode Enabled: Reference Voltage for BOR is from gpio1_anaOut (Test Mode	1	rw	0x0

8.2.13 GPIO bit control & configuration

GPIO		
Address	**Register Name**	**Description**

0x50018000	GPADATA	GPIO Port A Data
0x50018800	GPENA	GPIO Port Enables
0x50019000	GPAP03	GPIO Port A Pin 0-3 Control
0x50019004	GPAP74	GPIO Port A Pin 4-7 Control

8.2.13.1 GPADATA

0x50018000	GPADATA	^

GPIO Port A Data. bit[0] GPIO1 PIN, bit[1] GPIO2 PIN, bit[2] LIN_IN PIN, bit[3] LIN_OUT PIN, bit[4] GPIO3 PIN, bit[5] GPIO4 PIN, bit[6] GPIO5 PIN, bit[7] GPIO6 PIN

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0							

#	Field Name	Field Description	Width	Access	Reset
F0	GPADATA	Port A data. To aid in the efficiency of software, the GPIO ports allow for the modification of individual bits in the GPIO Data by using bits [7:0] of the address bus as a enable. In this manner, software drivers can modify individual GPIO pins in a single instruction without affecting the state of the other pins. This method is more efficient than the conventional method of performing a read-modify-write operation to set or clear an individual GPIO pin. To write all the bits at the same time use address offset of 0x03F.	8	dual	0xC

8.2.13.2 GPENA

0x50018800	GPENA	^

GPIO Port Enables.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	GPAENA	Enables the Clock-Gate, can be cleared to save power, if none of the GPIO functionality is required	1	rw	0x1

8.2.13.3 GPAP03

0x50019000 — GPAP03 ^

GPIO Port A Pin 0-3 Control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	F30	F29	F28	F27	F26	F25	F24	F23	F22	F21	F20	F19	F18	F17	F16	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F31	GPAACTDETFE[3]	LIN_OUT PIN activity fall status.	1	ro	N/A
F30	GPAACTDETRE[3]	LIN_OUT PIN activity rise status.	1	ro	N/A
F29	GPAACTDET[3]	LIN_OUT PIN activity interrupt.	1	ro	N/A
F28	GPACLR[3]	LIN_OUT PIN interrupt clear. Autoclear: inlcudes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F27	GPAFE[3]	LIN_OUT PIN falling edge enable.	1	rw	0x0
F26	GPARE[3]	LIN_OUT PIN rising edge enable.	1	rw	0x0

F25	GPAIE[3]	LIN_OUT PIN interrupt mask.	1	rw	0x0
F24	GPADIR[3]	NOT USED. SEE IOCTRL RxLIN_ena & TxLIN_ena.	1	rw	0x0
F23	GPAACTDETFE[2]	LIN_IN PIN activity fall status.	1	ro	N/A
F22	GPAACTDETRE[2]	LIN_IN PIN activity rise status.	1	ro	N/A
F21	GPAACTDET[2]	LIN_IN PIN activity interrupt.	1	ro	N/A
F20	GPACLR[2]	LIN_IN PIN interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F19	GPAFE[2]	LIN_IN PIN falling edge enable.	1	rw	0x0
F18	GPARE[2]	LIN_IN PIN rising edge enable.	1	rw	0x0
F17	GPAIE[2]	LIN_IN PIN interrupt mask.	1	rw	0x0
F16	GPADIR[2]	NOT USED. SEE IOCTRL RxLIN_ena & TxLIN_ena.	1	rw	0x0
F15	GPAACTDETFE[1]	GPIO2 PIN activity fall status.	1	ro	N/A
F14	GPAACTDETRE[1]	GPIO2 PIN activity rise status.	1	ro	N/A
F13	GPAACTDET[1]	GPIO2 PIN activity interrupt.	1	ro	N/A
F12	GPACLR[1]	GPIO2 PIN interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F11	GPAFE[1]	GPIO2 PIN falling edge enable.	1	rw	0x0
F10	GPARE[1]	GPIO2 PIN rising edge enable.	1	rw	0x0
F9	GPAIE[1]	GPIO2 PIN interrupt mask.	1	rw	0x0
F8	GPADIR[1]	GPIO2 PIN output enable.	1	rw	0x0
F7	GPAACTDETFE[0]	GPIO1 PIN activity fall status.	1	ro	N/A
F6	GPAACTDETRE[0]	GPIO1 PIN activity rise status.	1	ro	N/A

F5	GPAACTDET[0]	GPIO1 PIN activity interrupt.	1	ro	N/A
F4	GPACLR[0]	GPIO1 PIN interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F3	GPAFE[0]	GPIO1 PIN falling edge enable.	1	rw	0x0
F2	GPARE[0]	GPIO1 PIN rising edge enable.	1	rw	0x0
F1	GPAIE[0]	GPIO1 PIN interrupt mask.	1	rw	0x0
F0	GPADIR[0]	GPIO1 PIN output enable.	1	rw	0x0

8.2.13.4 GPAP74

0x50019004	GPAP74	^

GPIO Port A Pin 4-7 Control.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F31	F30	F29	F28	F27	F26	F25	F24	F23	F22	F21	F20	F19	F18	F17	F16	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F31	GPAACTDETFE[7]	GPIO6 PIN activity fall status.	1	ro	N/A
F30	GPAACTDETRE[7]	GPIO6 PIN activity rise status.	1	ro	N/A
F29	GPAACTDET[7]	GPIO6 PIN activity interrupt.	1	ro	N/A
F28	GPACLR[7]	GPIO6 PIN interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F27	GPAFE[7]	GPIO6 PIN falling edge enable.	1	rw	0x0

F26	GPARE[7]	GPIO6 PIN rising edge enable.	1	rw	0x0
F25	GPAIE[7]	GPIO6 PIN interrupt mask.	1	rw	0x0
F24	GPADIR[7]	GPIO6 PIN output enable.	1	rw	0x0
F23	GPAACTDETFE[6]	GPIO5 PIN activity fall status.	1	ro	N/A
F22	GPAACTDETRE[6]	GPIO5 PIN activity rise status.	1	ro	N/A
F21	GPAACTDET[6]	GPIO5 PIN activity interrupt.	1	ro	N/A
F20	GPACLR[6]	GPIO5 PIN interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F19	GPAFE[6]	GPIO5 PIN falling edge enable.	1	rw	0x0
F18	GPARE[6]	GPIO5 PIN rising edge enable.	1	rw	0x0
F17	GPAIE[6]	GPIO5 PIN interrupt mask.	1	rw	0x0
F16	GPADIR[6]	GPIO5 PIN output enable.	1	rw	0x0
F15	GPAACTDETFE[5]	GPIO4 PIN activity fall status.	1	ro	N/A
F14	GPAACTDETRE[5]	GPIO4 PIN activity rise status.	1	ro	N/A
F13	GPAACTDET[5]	GPIO4 PIN activity interrupt.	1	ro	N/A
F12	GPACLR[5]	GPIO4 PIN interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F11	GPAFE[5]	GPIO4 PIN falling edge enable.	1	rw	0x0
F10	GPARE[5]	GPIO4 PIN rising edge enable.	1	rw	0x0
F9	GPAIE[5]	GPIO4 PIN interrupt mask.	1	rw	0x0
F8	GPADIR[5]	GPIO4 PIN output enable.	1	rw	0x0
F7	GPAACTDETFE[4]	GPIO3 PIN activity fall status.	1	ro	N/A

F6	GPAACTDETRE[4]	GPIO3 PIN activity rise status.	1	ro	N/A
F5	GPAACTDET[4]	GPIO3 PIN activity interrupt.	1	ro	N/A
F4	GPACLR[4]	GPIO3 PIN interrupt clear. Autoclear: includes a synchronous reset signal which clears the register on the cycle following write.	1	wo	0x0
F3	GPAFE[4]	GPIO3 PIN falling edge enable.	1	rw	0x0
F2	GPARE[4]	GPIO3 PIN rising edge enable.	1	rw	0x0
F1	GPAIE[4]	GPIO3 PIN interrupt mask.	1	rw	0x0
F0	GPADIR[4]	GPIO3 PIN output enable.	1	rw	0x0

8.2.14 General purpose timer0

TIMER0		
Address	**Register Name**	**Description**
0x50020000	COUNT	Count
0x50020004	CFG	Config

0x50020000	COUNT	^
Count.		

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

F0					
#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F0	COUNT	Count.	32	rw	0x0

0x50020004	CFG	^

Config.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	**Field Name**	**Field Description**	**Width**	**Access**	**Reset**
F0	ENA	Enable.	1	rw	0x0

8.2.15 General purpose timer1

TIMER1		
Address	**Register Name**	**Description**
0x50020008	COUNT	Count
0x5002000C	CFG	Config

0x50020008	COUNT	^

Count.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	COUNT	Count.	32	rw	0x0

0x5002000C	CFG	^

Config.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	ENA	Enable.	1	rw	0x0

8.2.16 General purpose timer 2

TIMER2		
Address	**Register Name**	**Description**
0x50020010	COUNT	Count
0x50020014	CFG	Config

0x50020010	COUNT	^

Count.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	COUNT	Count.	32	rw	0x0

0x50020014	CFG	^

Config.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0

#	Field Name	Field Description	Width	Access	Reset
F0	ENA	Enable.	1	rw	0x0

8.2.17 MCU Watchdog Timer

WDT1

Address	Register Name	Description
0x50020018	CFG	Config
0x5002001C	KEY	Key

0x50020018 CFG ^

Config.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F3		F2	F1	F0

#	Field Name	Field Description	Width	Access	Reset
F3	PRESET	Preset. Defines the watchdog timeout period. It means that the WDT internal counter will count from 0 to the prescaler value at the system clock speed and trigger if not cleared. For instance, a system running from a 30MHz Crystal with WDTPRES[1I0] = 10 will trigger the WDT after approximately 0.14 seconds if not cleared properly and in time by the application. 0x0: 2^13 / System Clock 0x1: 2^19 / System Clock 0x2: 2^22 / System Clock 0x3: 2^32 / System Clock	2	rw	0x0
F2	RSTFLAG	Reset flag. This flag is set by the system at the initialization if the initialization was caused by a reset triggered by the WDT. The bit can be cleared by the application.	1	rw	0x0
F1	RSTEN	Reset enable. If enabled a WDT time-out will force the microcontroller to reset. This	1	rw	0x0

		bit can be asserted but it cannot be de-asserted.			
F0	ENA	WDT Enable. This bit can be asserted but it cannot be de-asserted. It means that once the WDT is enabled it cannot be turned off until a Reset or Power-On Reset occurs.	1	rw	0x0

0x5002001C KEY ^

Key. Writing the sequence CLEAR, KEY0, KEY1 to this register will clear (pet) the watchdog - preventing it from timing out and resetting the system.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	KEY	Key. To clear the WDT counting the following words must be written in this order and without any other instruction between then: 0x3C570001 0x007F4AD6	32	rw	0x0

8.2.18 Flash Programming/Erase Control

FLASH		
Address	**Register Name**	**Description**

0x50020020	FLADDR	Destination address for flash write / erase operation
0x50020024	FLWRDT	Flash data to be written
0x50020028	UNLBWR	Flash data unlock register
0x5002002C	BWRSTRT	Flash write start register
0x50020030	UNLSER	Flash sector erase unlock register
0x50020034	SERSTRT	Flash sector erase start register
0x50020040	FLSCTRL	Flash control register
0x50020044	FLSCP	Flash code protection register
0x50020050	FLS_UNLOCK_CTRL_OP	Flash Unlock Control Operation Register
0x50020054	CTRL_OP	Flash Control Operation Register
0x50020058	TRIM	Flash Trim Register

8.2.18.1 FLADDR

0x50020020	FLADDR	^

Destination address for flash write / erase operation.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0																

#	Field Name	Field Description	Width	Access	Reset
F0	ADDR	Target address for write/erase operation. In byte writes, this is the read address of the flash to be written to. In erase modes, it is a read address inside the sector	17	rw	0xFFFF

		to be erased. This register must be written in the correct sequence or the operation will fail.			

8.2.18.2 FLWRDT

0x50020024	FLWRDT	^

Flash data to be written.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	DATA	Content to be written into the targeted address. This register must be written in the correct sequence or the operation will fail.	32	rw	0x0

8.2.18.3 UNLBWR

0x50020028	UNLBWR	^

Flash data unlock register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	UNLOCK_WRITE	Control register to unlock write. A value of 0x55555555 must be written to this address at the correct point in the write sequence or the operation will fail.	32	rw	0x0

8.2.18.4 BWRSTRT

0x5002002C	BWRSTRT	^

Flash write start register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#		Field Name	Field Description	Width	Access	Reset
F0		WRITE_START	Control register to start a write. A value of 0xAAAAAAAA must be written to this address at the correct point in the write sequence or the operation will fail.	32	rw	0x0

8.2.18.5 UNLSER

0x50020030	UNLSER	^

Flash sector erase unlock register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	UNLOCK_ERASE	Control register to unlock a sector erase. A value of 0x66666666 must be written to this address at the correct point in the sector erase sequence or the operation will fail.	32	rw	0x0

8.2.18.6 SERSTRT

0x50020034	SERSTRT	^

Flash sector erase start register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	ERASE_START	Control register to commit a sector erase. A value of 0x99999999 must be written to this address at the correct point in the sector erase sequence or the operation will fail.	32	rw	0x0

8.2.18.7 FLSCTRL

0x50020040	FLSCTRL	^

Flash control register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F0	

#	Field Name	Field Description	Width	Access	Reset
F0	CTRL	Number of wait states used in the reading process. Each read from flash memory will take number of cycles equal to 1+RWC to complete.	2	rw	0x1

8.2.18.8 FLSCP

0x50020044	FLSCP	^

Flash code protection register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	CODE_PROT	Code Protection / SerialWire Lockout Control Code protection control register. Write a value of 0xF2E11047 to disable the SerialWire interface. Write 0x00000000 to enable it. This allows the user program to disable the SerialWire interface to prevent unauthorized debug access to the part. NOTE1: This register does not lock the Flash Memory against read/write/erase by the applications program. Instead what it does is to disable all communications with the debug interface, therefore preventing any external attack. The application code is still able to modify the flash content. NOTE2: Upon Power-On Reset or Normal Reset the system disables the communication for a small time interval (8192 clock cycles). If the application needs to be protected it is mandatory to set this register with the appropriate code in the beginning of the initialization process and before the internal hardware enable the debug communication.	32	rw	0x0

8.2.18.9 FLS_UNLOCK_CTRL_OP

0x50020050	FLS_UNLOCK_CTRL_OP	^

Flash Unlock Control Operation Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F0																															

#	Field Name	Field Description	Width	Access	Reset
F0	UNLOCK_CTRL_OP	Flash Control Operation Register Unlock value. 0xACDC_1972 needs to be written in this register to unlock the Control Operation Register access. When this register is read, it returns the state of the lock: 0: The Control Operation Register is locked. The Control Operation Register (FLASH_CTRL_OP) cannot be written. 1: The Control Operation Register is unlocked. The Control Operation Register (FLASH_CTRL_OP) can be written. Note: After each write to the FLASH_CTRL_OP register, the state of the lock is cleared and the pattern needs to be written again to allow a new configuration of the register.	32	rw	0x0

8.2.18.10 CTRL_OP

0x50020054 **CTRL_OP** ^

Flash Control Operation Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	F1		F0

#	Field Name	Field Description	Width	Access	Reset
F1	SIZE	SIZE of the write operation. Refer to data sheet for more information of the use of this field.	2	rw	0x0
F0	CHIP	CHIP bit. This bit is only used during the Erase operation. It allows the system to erase more than one sector. 0: The Erase operation will only erase the sector selected by the FLASH_ADDR register value. 1: The Erase operation will erase the full main array of the flash.	1	rw	0x0

8.2.18.11 TRIM

0x50020058	TRIM	^

Flash Trim Register.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	F17	F16	F0															

#	Field Name	Field Description	Width	Access	Reset
F17	SLEEPDEEP_CFG	Deep Sleep VDD_IO configuration. This register will be automatically populated with the value stored in the NVR sector 1 (@0001_0000). When set, the system will NOT be reset if VDD_IO is going away during Deep Sleep mode. Otherwise (0), the system is reset if VDD_IO is removed.	1	rw	0x0
F16	SDIO_TIMING_CFG	SDIO interface timing configuration. This register will be automatically populated with the value stored in the NVR sector 1 (@0001_0000). When set, the SDIO/INT signals are captured on the rising edge of CLK. When cleared, these data are captured on the falling edge of CLK	1	rw	0x1
F0	OSC_TRIM	Oscillator Trim Value. This register will be automatically populated with the value stored in the NVR sector 1 (@0001_0000).	16	rw	0x86

9 DEVICE FUNCTIONAL DESCRIPTION

9.1 MCU FEATURES

9.1.1 MCU Core

The chip implements one ARM Cortex M0 core.

Additional documentation on ARM Cortex-M0 32 bits microcontroller can be found at

http://www.arm.com/products/processors/cortex-m/cortex-m0.php

9.1.2 System Memory (SRAM)

MCU core implements 16kbytes of SRAM. MCU can execute codes from the SRAM memories.

9.1.3 Flash Non Volatile Memory

MCU implements a Programmable Flash Memory with x32 configuration, sector and chip erase and byte program capability. It integrates five 512bytes nonvolatile registers (NVR) sectors.

In normal operation the ARM core fetches instructions (or data permanently stored) from the Flash memory but it is also possible for a program to alter the content of the flash memory. The following operations can be performed in the Flash Memory:

- Byte Write
- Sector Erase
- Block Erase
- Code Protect

For a description of the flash memory registers, please refer to the product register map. Here is a simple description of the basic features supported:

- Registers support to write/erase data to a byte, sector address
- Support programmable read wait states*
- Support system clock divider for write/erase functions
- Protection mechanism to unlock flash memory write and start flash memory byte-write
- Protection mechanism to unlock flash memory sector erase

* The design is implemented such that the timings associated with the flash macro meet the maximum speed of the system clock requirements.

9.1.4 Interrupt vectors

The first 148 bytes of Flash Memory are organized following the standard created by ARM. In this standard the Address 0x00000 contains the top-of-stack address (four bytes). The following addresses contain interrupt vectors used by the microcontroller:

Table 9 Interrupt Vector

Vector Name	Address	Comments
STACK_VALUE	0x00000	Typically set to 0x20000FFFF (Top of SRAM)
Reset_Handler	0x00004	Reset routine entry
Reserved	0x00008	Reserved. No NMI implemented.
HardFault Handler	0x0000C	
Reserved	0x00010 to 0x00028	
SVC_Handler	0x0002C	
Reserved	0x00030-0x00034	
PendSV_Handler	0x00038	
SysTick_Handler	0x0003C	
WULIN_Handler,	0x00040	Wake Up LIN Slave

IOCTRLA_Handler,	0x00044	LINS/LINM TxD Dominant Timeout
WUTIMER_Handler,	0x00048	Wake Up Timer
BOR_Handler,	0x0004C	Brown out event
WatchdogA_Handler,	0x00050	ASIC watchdog timeout
UV_Handler,	0x00054	Under voltage event
OV_Handler,	0x00058	Over voltage event
LINS_Handler,	0x0005C	LIN Slave bus event
ADC_Handler,	0x00060	ADC data ready
PWM_Handler,	0x00064	PWM event
LINM_Handler,	0x00068	LIN Master bus event
GPIO_Handler,	0x0006C	GPIO Interrupts
WULINM_Handler,	0x00070	Wake Up LIN Master
OVTEMP_Handler,	0x00074	Over Temperature event
Reserved	0x00078	Reserved
Lullaby_Handler,	0x0007C	Software Interrupt
Timer0_Handler	0x00080	
Timer1_Handler	0x00084	
Timer2_Handler	0x00088	
Watchdog_Handler	0x0008C	
BTE_Handler	0x00090	Block Transfer – Contact indie to get more information.
Reserved	0x00094	

All other addresses in the flash memory can be used for the user's program.

The meanings of the standard interrupt vectors (Provided with the ARM Cortex M0 core) are defined in ARM's documentation. One of the sources of information is:

http://infocenter.arm.com/help/topic/com.arm.doc.dui0497a/DUI0497A_cortex_m0_r0p0_generic_ug.pdf

9.1.5 Interrupt Enabling/Disabling Process

Cortex-M0 implements a NVIC (**N**ested **V**ector **I**nterrupt **C**ontroller) peripheral capable of handling up to 16 peripheral's interrupts. Upon reset the microcontroller can answer only to Reset, NMI (Non-Maskable Interrupt) and Hard-Fault interrupts/exceptions. All other interrupts must be enabled. To enable and disable the interrupts the user must use access the ISER (Interrupt Set Enable Register) and ICER (Interrupt Clear Enable Interrupt) registers associated with the desired interrupt.

NOTE: Both inline functions and all parameters are defined in the product_file.h file, which must be included in the source files. Besides that the product_file.h file contains a list of available interrupts. The format of this list is as follows:

```
typedef enum IRQn
{
 //******  Cortex-M0 Processor Exceptions Numbers ***************************
 NonMaskableInt_IRQn       = -14,    // Non Maskable Interrupt
 HardFault_IRQn            = -13,    // Hard Fault Interrupt
 SVCall_IRQn               = -5,     // SV Call Interrupt
 PendSV_IRQn               = -2,     // Pend SV Interrupt
 SysTick_IRQn              = -1,     // System Tick Interrupt

 //*****  CM0IKMCU Cortex-M0 specific Interrupt Numbers **********************
 IRQ04_IRQn                = 0,      // Product specific
 IRQ04_IRQn                = 1,      // Product specific
 IRQ04_IRQn                = 2,      // Product specific
 IRQ04_IRQn                = 3,      // Product specific
```

```
  IRQ04_IRQn            = 4,     // Product specific
  IRQ05_IRQn            = 5,     // Product Specific
  IRQ06_IRQn            = 6,     // Product Specific
  IRQ07_IRQn            = 7,     // Product Specific
  IRQ08_IRQn            = 8,     // Product Specific
  IRQ09_IRQn            = 9,     // Product Specific
  IRQ10_IRQn            = 10,    // Product Specific
  IRQ11_IRQn            = 11,    // Product Specific
  IRQ12_IRQn            = 12,    // Product Specific
  IRQ13_IRQn            = 13,    // Product Specific
  IRQ14_IRQn            = 14,    // Product Specific
  IRQ15_IRQn            = 15,    // Product Specific
  TIMER0_IRQn            = 16,    // Timer 0
  TIMER1_IRQn            = 17,    // Timer 1
  TIMER2_IRQn            = 18,    // Timer 2
  WATCHDOG_IRQn          = 19     // Watchdog timer
} IRQn_Type;
```

9.1.6 Flash Code protection

The controlled access to the flash content is based on disabling all communications with the debug interface, therefore preventing any external attack. Hence, the application code is still able to modify the Flash content.

Upon Power-On Reset or Normal Reset, MCU core disables the communication with the debug interface for a small time interval (8192 system clock cycles). If the application needs to be protected it is mandatory to set the protection register with the appropriate code in the beginning of the initialization process and before the internal hardware enable the debug communication. In other words, if during this time interval the protection register is loaded with a specific pattern, then the communication remains disabled after the end of this interval and stays disabled until this register is loaded with a different pattern. To allow for debug communication the application has only to write a different value in the lock register.

If a part is protected, the emulator can still erase and program the part, but first it will be required to erase the Flash content, therefore protecting it.

9.1.7 Systick Timer

This timer is an optional peripheral created by ARM and implemented in the Cortex M0 160/8. It is fully described in the Cortex-M0 Devices Generic User Guide (Chapter 4.4 Optional System Timer, Systick) found at:

http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.dui0497a/Babieigh.html

9.1.8 Timers (0, 1 and 2)

The MCU implements three identical timers: Timer0, Timer1 and Timer2. All three timers operate using the system clock as clock source. They increment at the system clock rate starting from the loaded value in the counter until they roll over from 0xFFFFFFFF to 0x00000000. At this point an interrupt is generated if enabled. The interrupt routine is responsible for reloading the value if needed as this timer does not auto-reload the original content.

9.1.9 Watch Dog Timer

The MCU implements a WDT (**W**atch **D**og **T**imer) that can operate in one of two ways:

- Interrupt Mode: In the event of a WDT rollover an interrupt will be generated.
- Reset Mode: In the event of a WDT rollover the microcontroller will reset.

The WDT supports Reset, Enable, status/flag and clear functions. It integrates a pre-scaler that can divide the system clock by 2^{13}, 2^{19}, 2^{22} or 2^{32}. It means that the WDT internal counter will count from 0 to the pre-scaler value at the system clock speed and trigger if not cleared.

For instance, a system running from a 30MHz system clock and 2^{22} pre-scaler value will trigger the WDT after approximately 0.14 seconds if not cleared properly and in time by the application.

9.1.10 MCU Core to ASIC interface

The ASIC die will be communicating to the indie Cortex M0 through a proprietary interface. The interface used with mcu should be fully kept as is to enable any swap between ASIC die and MCU die.

9.2 ASIC FEATURES

9.2.1 Power on sequence

Figure 6 shows the power on sequence , VDD3V3/ VDD1V5 connect to the external 4.7uF capacitor.

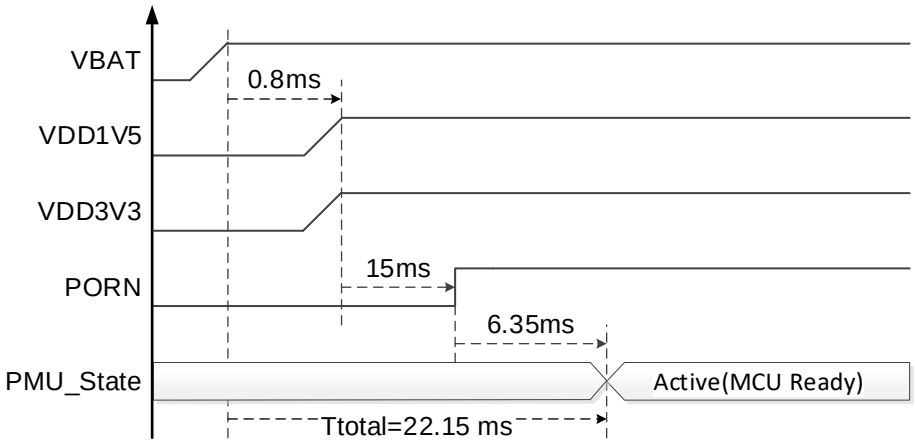


Figure 6 power on sequence

ASIC has an On-chip Brown-out Detection (BOD) circuit for monitoring the VCC level during operation by comparing it to a fixed trigger level. The trigger level for the BOD can be selected by the BOR3V3THRESH / BOR1V5THRESH. The trigger level has a hysteresis to ensure spike free Brown-out Detection.

The BOD circuit can be enabled/disabled by the fuse BOR_EN. When the BOD is enabled and BOR ACTION is configured as Hard reset, and VDD_3V3/ VDD_1V5 decreases to a value below the trigger level (BOR_3V3_thre/ BOR_1V5_thre - in Figure 7), the Brown-out Reset(BORN) is activated. When VCC increases above the trigger level (BOR_3V3_thre/ BOR_1V5_thre - in Figure 7), the BORN is released.

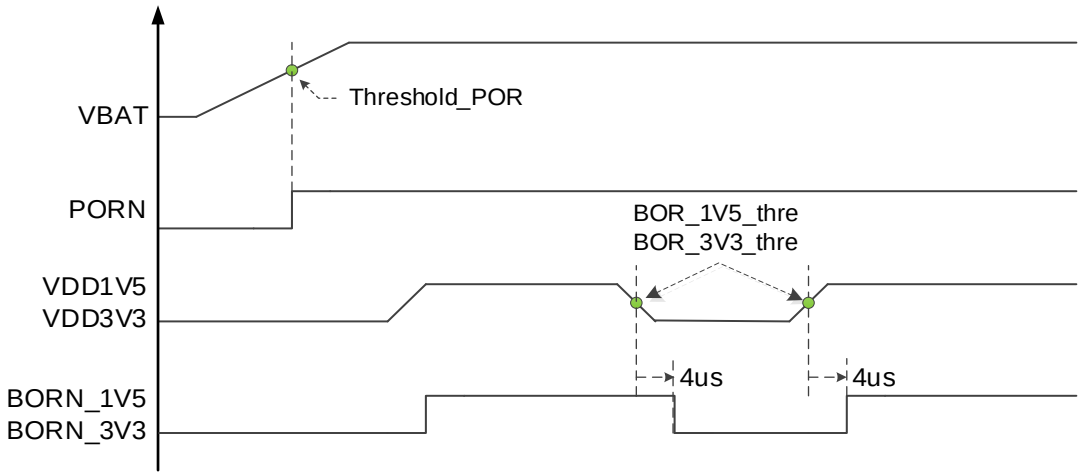


Figure 7 BORN Generation

9.2.2 Clock Generation

Two clock sources are integrated in the device. The system clock is based on a RC network and will be trimmed to meet the accuracy requirements specified in the EC Table. Additionally, an auxiliary clock will be used during Hibernate.

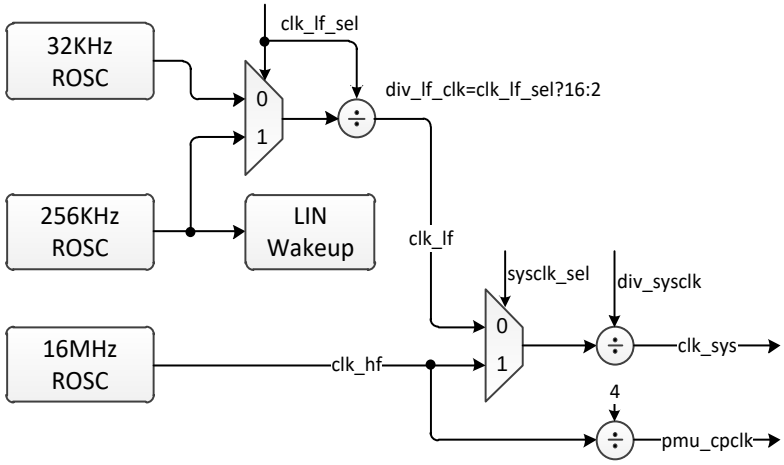


Figure 8 Clock Generation

9.2.3 Reset

Both ASIC and MCU integrates Power on Reset (POR) circuitry: MCU POR monitors its input supply and generate a reset every time the MCU supply is recycled. ASIC POR monitors the main 3V3 LDO supply and generate a reset every time the LDO supply is recycled. Both POR maintain their output reset active as long as the monitored supply voltage is not above the minimum supply level to ensure safe logic operation of the Power Management Unit including the necessary analog features such as clock generator, bandgap, etc…This level is hardcoded and process technology dependent.

Additionally, the ASIC integrates Brown Out (BOR) circuit detectors that are configurable by SW (enable/disable as well as threshold programmable for the main ASIC core supply) and are actively monitored by the ASIC power management unit (PMU). In case any BOR is triggered, the PMU can be configured to either do the following (per BOR blocks).

- trigger a system reset
- generate an interrupt to the MCU for further actions.
- do nothing

The table below show the BOR levels settings for both VDD3P3 (ASIC Core supply) and VDD1P5 (MCU Core Supply). The * are the default settings values after reset and do not need to be changed as the thresholds are guaranteed to provide safe margin for full operation across PVT.

BOR Setting <3:0>	**BOR Level VDD3P3**		**BOR Level VDD1P5**	
	Threshold [V]	VBAT [V]	Threshold [V]	VBAT [V]
0	2.10	4.40	1.376*	5.1
1	2.10	4.40	1.344	5.03
2	2.10	4.40	1.315	4.95
3	2.32	4.47	1.285	4.88
4	2.39	4.55	1.413	5.19
5	2.46	4.63	1.449	5.28
6	2.56*	4.73	1.484	5.37
7	2.65	4.83	1.523	5.47
8	2.74	4.94	1.568	5.59
9	2.84	5.05	1.608	5.71
A	2.96	5.18		
B	3.08	5.32		
C	3.21	5.48		
D				
E				

F				

Table 10 BOR Trigger Level [* reset default]

Finally, the MCU watchdog timer (if configured to do so) or a reset instruction can reset the MCU logic while on the ASIC side the watchdog timer (if configured to do so) or a reset register write can reset the ASIC system.

The block diagram below illustrates the possible triggers of a reset on both side of the design: ASIC and MCU.

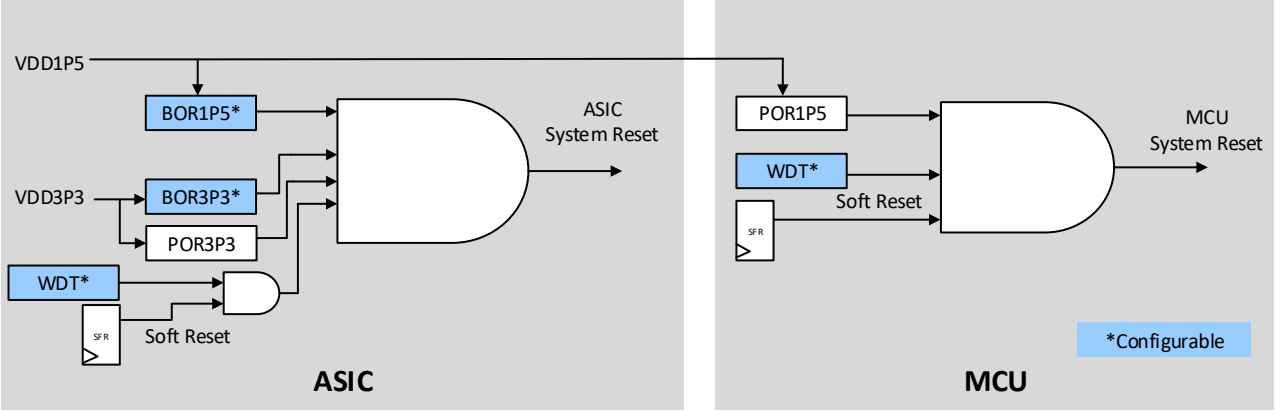


Figure 9 System Reset sources (Reset active LOW)

9.2.4 PMU and Load Dump Protect circuits

ASIC integrates battery monitoring functionality that will detect load dump events occurring at the battery supply pin. An analog comparator will detect over voltage transients after going through a load dump limitation circuit. The protection circuit can handle DC voltage up to 45V and will limit these to maximum of *Over Voltage Threshold* nominal, therefore the comparator will detect any over voltage transients at the battery pin beyond that threshold. The circuit will generate a digital output signal to be filtered and sent to the interrupt controller. The circuit will be active during normal operation mode – not during Hibernate condition.

The voltage regulators themselves are supplied by VBAT directly and sustain DC level of load dump voltages.

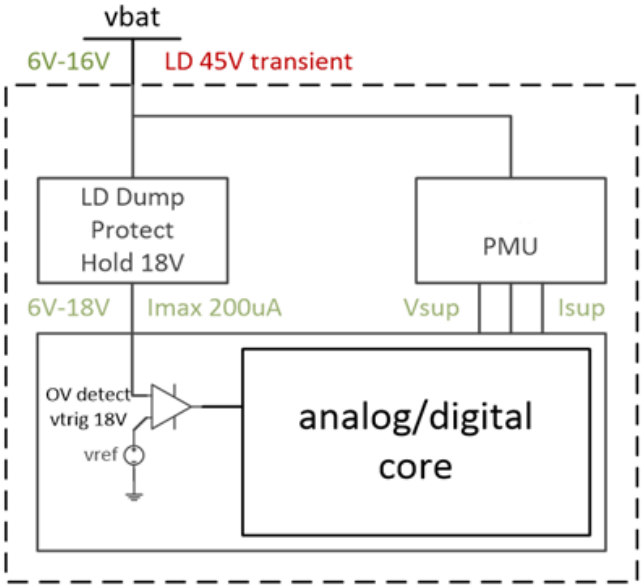


Figure 10 Load Dump Protect

9.2.5 LIN Interface

9.2.5.1 LIN Transceiver

Supports LIN Protocol Controller according to LIN 2.x and SAE J2602 (rev J2602-1_201211). The IC contains two integrated PHYs (One for Slave and the other for Master) for low speed vehicle serial data network communication using the LIN protocol.

Notice that LIN Master PHY is disconnected from LIN Master controller is the internal LIN Switch is enabled.

9.2.5.1.1 LIN RxD Debounce

For preventing RxD spikes in case of RF interferences and automotive pulses, two digital glitch filters are integrated in the data pathes of LIN RxD.

Debounce thresholds for low to high and high to low can be programmable independently (See LINSGFCONF & LINMGFCONF).

$$T_{thres} = \left(T_{hfosc}\right) \times LINDBNCTHRESx$$

For instance, the default DBNCTHRES value is 0x30 and HFOSC freq is 16MHz.Thus the default debounce threshold is 62.5ns * 48 = 3 us.

9.2.5.1.2 LIN TxD Timeout Monitor

Two TxD Timout monitors are integrated to prevent dominant bus due to internal malfunction. LIN TX is controlled by TxD signal from LIN controller or GPA(Selected by bit LINS_HWMODE in 8.2.11.7). If TxD is stuck at low over a specified TxD timeout time due to a crash of MCU/GPA/LIN Controller, the integrated TxD monitor will switch off the LIN TX output automatically until a low to high transition of TxD.

9.2.5.1.3 Short LIN Bus to Ground

If the bus idle timeout monitor detects the bus is shorted to ground (See bit BUS_IDLE_TIMEOUT_DOMINANT in 8.2.8.17), LIN Slave's 30K pullup will be automatically switched off to prevent a fast discharge of the car battery.

If enabled, the feature is always on even the chip is in hibernate mode.

9.2.5.1.4 External LIN Transceiver Mode

In this mode, the internal LIN transceiver is bypassed and LIN Slave controller's RxD/TxD can be connected with an external transceiver through GPIO3/4 or GPIO5/6(See HWMODE bits from 8.2.11.3 to 8.2.11.6); LIN Master controller's RxD/TxD can be connected with an external transceiver through GPIO1/2(See HWMODE bits from 8.2.11.1 to 8.2.11.2).

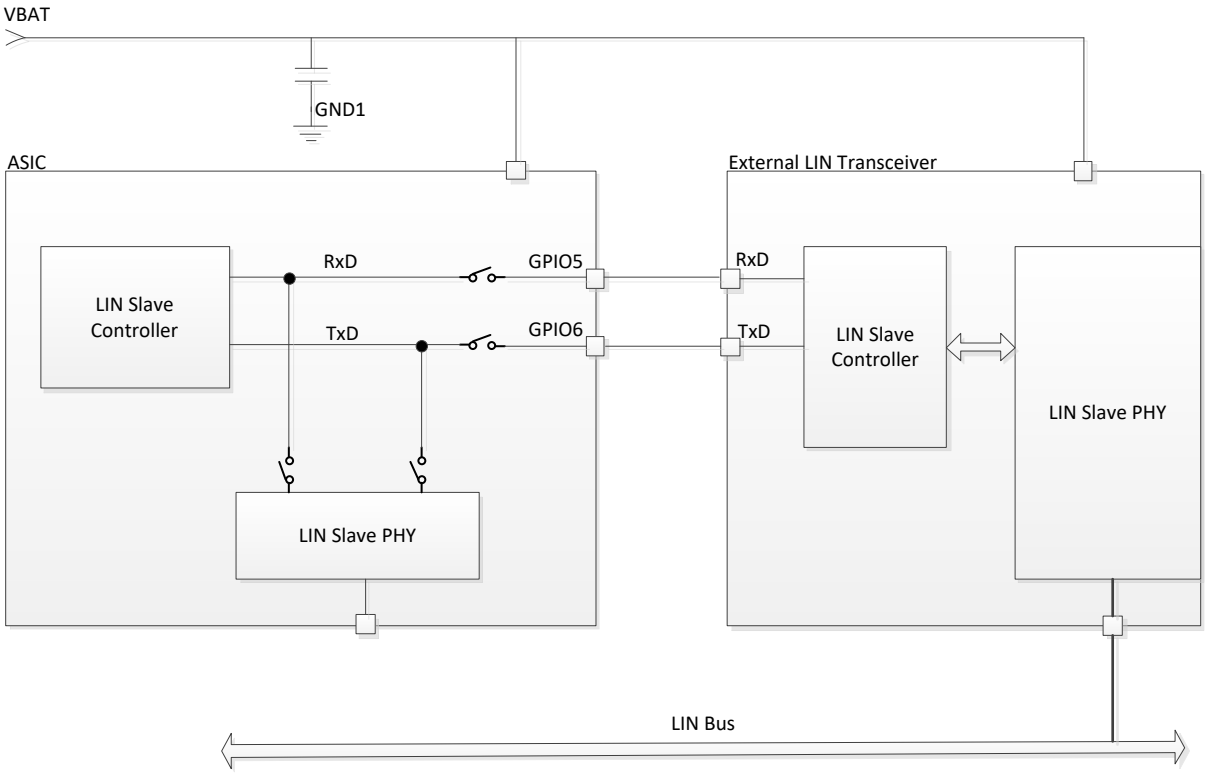


Figure 11 External LIN Transceiver Connection

9.2.5.2 LIN controller

The IC contains two LIN cores. One is for LIN Slave and the other is for LIN Master. The LIN core is a communication controller that performs serial communication. It implements the datalink layer of the LIN Protocol Specification. LIN uses a single master / multiple slave concept for the message transfer between nodes of the LIN network. The LIN controller core comprises an interface to connect a micro controller that accesses the LIN core registers to control the transmission and reception of message frames.

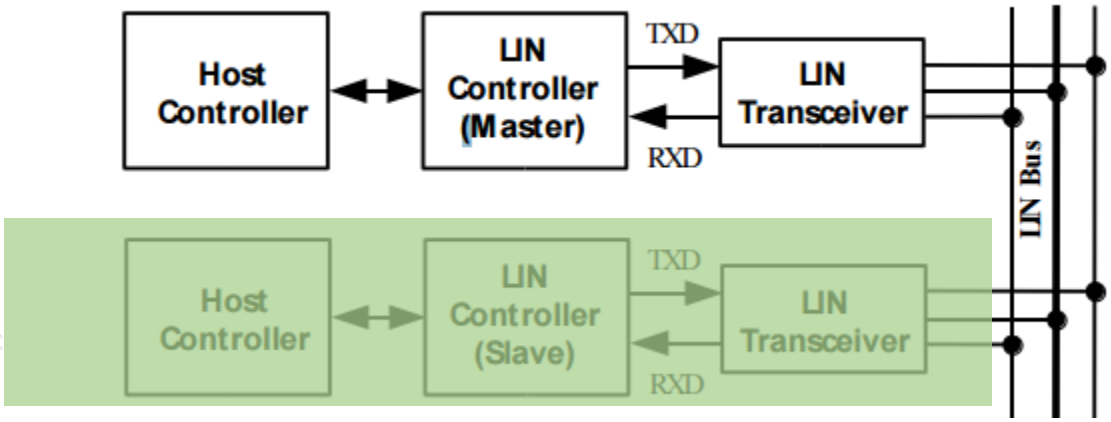


Figure 12 LIN System

Features:

- One LIN Slave Controller
  - Support of LIN specification 2.2A/SAE J2602
  - Backward compatibility to LIN 1.3
  - Supports LIN auto-addressing through an internal LIN switch.
- One LIN Master Controller
  - Only available when the internal LIN switch is not used.
  - Only supports auto-baudrate LIN Slaves.
- Programmable data rate between 1 Kbit/s and 20 Kbit/s (for master)
- Automatic bit rate detection (for slave)
- 8-byte data buffer
- 8-bit host controller interface
- Fully synchronous design, available in VHDL or Verilog, completely synthesizable
- Support auto addressing
  - Note: Node configuration and diagnostics implemented by the host controller

9.2.5.2.1 Data Length Register and Enhanced Checksum

The host controller has to define the length of the data field of the current LIN frame by adjusting the DATA LENGTH register. If the data length bits[3:0] are loaded with the value “1111b” the length of the data field is decoded from Bit 5 and 4 of the identifier register (ID) according to table below (e.g. compatibility to LIN specification 1.1). Otherwise the amount of data bytes can be written directly to the DATA LENGTH register (supported values are 0...8).

Table 11 ID bits and number of bits

ID (Bit 5)	ID (Bit 4)	Number of Bytes in the data field
0	0	2
0	1	2
1	0	4
1	1	8

The LIN core supports classic checksum (Spec 1.3, inverted eight bit sum with carry over all data bytes) and enhanced checksum (Spec. 2.0, inverted eight bit sum with carry over all data bytes and protected identifier). The host controller has to set the checksum type used in the current frame by adjusting Bit ENCHK in the data length register (‘1’ for enhanced checksum, ‘0’ for classic checksum).

9.2.5.2.2 Timing Settings for "Wake up Repeat Time" and "Bus Inactivity Time"

The time for repeating of wake up because of no reaction on the bus and for go to sleep because of inactivity on the bus can be optionally written by the host controller to registers WUPREPEAT and BUSINACTIVE (address 0x0F).

Table 12 LIN Inactivity Time

BUSINACTIVE [1:0]	LIN Inactivity Time (sec.)
00	4*
01	6
10	8
11	10

Table 13 LIN Wake-Up Repeat Time

WUPREPEAT [1:0]	LIN Wake-Up Repeat Time (msec.)
00	180*
01	200
10	220
11	240

9.2.5.2.3 Bit Time Settings

The Bit rate of the LIN system has to be defined in the bit timing registers.

Table 14 Bit Timing Related Registers

Name	Description	Width(bits)
BTDIV	Bit time divider integer value	9
PRESCL	Clock Prescaler	2

The LIN bit rate *f*bit can be calculated from system clock *f*clk and bit timing registers according to the following general equation:

$$f_{bit} = \frac{f_{clock}}{2^{prescl} * bt\_div * (bt\_mul + 1)}$$

Note that the procedure of adjusting the bit timing registers is different between master and slave. For the slave controller, the Bit timing register adjustment of slave is the following:

The steps for adjusting the bit timing registers of the LIN slave are explained below.

Note: Register bt_mul does not exist in the slave. The LIN core slave synchronizes to any bit rate between 1 Kbit/s and 20 Kbit/s. Nevertheless, the bit timing registers have to be adjusted to adapt the LIN core to the used system clock frequency.

- Setting up the pre-scaler register depending on system clock according to the following equation; the value has to be rounded down to the next integer value:

$$prescl = \ln\left(\frac{f_{clock}}{20KHz * 200}\right) * \frac{1}{\ln 2}$$

- Adjusting the bit time divider depending on system clock and pre-scaler according to the following equation; the value has to be rounded down to the next integer value:

$$bt\_div = \frac{f_{clock}}{2^{prescl} * 20KHz}$$

Table 15 Sample value for setting up bit timing registers

System Clock	PRESCL	BTDIV
8MHz	1	200

12MHz	1	300
16MHz	2	200

9.2.5.2.4 Controlling the LIN core (slave) by a host controller

The first step before transmitting messages with the LIN core is setting up the bit rate of the LIN system. For that, the host controller has to load the bit time registers. After that, the message transfer can be started. The LIN core slave detects the header of the message frame sent by the LIN master and synchronizes its internal bit time to the master bit time. An interrupt to the host controller is requested after the reception of the IDENTIFIER FIELD, after the reception of a wakeup signal (if the slave is in sleep mode), when an error is detected or when the message transfer is completed.

The following steps have to be done by the host controller when an interrupt is requested.

1) Check bit DATAREQ in the status register (it is 1 when the IDENTIFIER FIELD has been received). Proceed with the following if DATAREQ is set else proceed with step 2.

    a. Load the identifier from the ID register and process it.
    b. Adjust the bit TRANSMIT in the control register (“1” - if the current frame is a transmit operation for the slave, “0” – if the current frame is a receive operation for the slave).
    c. Load the data length in the data LENGHT register (number of data bytes or value “1111b” if the data length should be decoded from the identifier) and set the checksum type (enhanced checksum (Bit ENHCHK = ‘1’) or classic checksum (Bit ENHCHK = ’0’)).
    d. Load the data to transmit into the data buffer (for transmit operation only).
    e. Set the bit DATAACK in the control register.

Note 1: Steps a..e have to be done during the IN-FRAME RESPONSE SPACE, if the current frame is a transmit operation for the slave; otherwise a timeout will be detected by the master. If the current frame is a receive operation for the slave, steps a..e have to be finished until the reception of the first byte after the IDENTIFIER FIELD. Otherwise, the internal receive buffer of the slave core will be overwritten and a timeout error will be detected in the slave core.

Note 2: If the host controller of the slave detects an unknown identifier (e.g. extended identifier) it has to write a ‘1’ to bit “stop” in control register instead of setting bit DATAACK (steps b .. e can be skipped). In that case the LIN core slave stops the processing of the LIN communication until the next SYNC BREAK is received.

2) Check bit ERROR in the status register. Perform error handling and proceed with step 6 if bit ERROR is set else proceed with step 3.

Note 3: Bit TIMEOUT in the error register and bit WAKEUP in the status register are set if the slave has sent a wakeup signal but the master did not respond within 150ms.

3) Check bit BUSIDLETIMEOUT in the status register and activate the sleep mode by setting bit SLEEP in the control register if BUSIDLETIMEOUT is set.
4) Check bit WAKEUP in the status register (it is set if the slave has received a wakeup signal). If WAKEUP is set proceed with step 6 else proceed with step 4.

Note 4: Bit COMPLETE in the status register is not changed when a wakeup signal is transmitted or received. Therefore, bit WAKEUP has to be checked before bit COMPLETE

5) Check bit COMPLETE in the status register (it is set if the transmission was successful). If COMPLETE is set and the current frame was a receive operation for the slave, load the received data bytes from the data buffer.
6) Set the bits RSTINT (reset interrupt) and RSTERR (reset error) in the control register to reset the interrupt request and the error flags.

9.2.5.2.5 Sleep Mode and Wakeup

To reduce the systems power consumption the LIN Protocol Specification defines a Sleep Mode. The message used to broadcast a Sleep Mode request has to be started by the host controller of the LIN core master in the same way as a normal transmit message. The host controller of the LIN core slave has to decode the Sleep Mode Frame from Identifier and data bytes. After that, it has to put the LIN slave node into the Sleep Mode by setting bit SLEEP in the control register. If bit SLEEP in the control register of the LIN core slave is not set and there is no bus activity for 4 s to 10 s (specified bus idle timeout), bit SLEEP & BUSIDLETIMOUT are set and an interrupt request is generated. After that application has to understand that the LIN bus is in Sleep Mode. The bus inactivity time which should be defined as bus idle timeout for the slave can optionally set to values 4s, 6s, 8s or 10s as possible accordingly with specification 2.2A.

After receiving a Wakeup signal from the master or any slave node a wakeup request is generated, the host controller terminates the Sleep Mode of the LIN bus by clearing bit SLEEP in the control register.

Notice that don’t enter hibernate mode when bit SLEEP = 0, because in this state dominant signal will not be taken as a wakeup request.

To send a Wakeup signal, the host controller of the LIN core has to set the bit WAKEUPREQ in the control register. After successful transmission of the wakeup signal with the LIN core master the WAKEUP bit in the status register of the sending LIN core master is set and an interrupt request is generated. The LIN core slave does not generate an interrupt request after successful transmission of the Wakeup signal but it generates an interrupt request if the master does not respond to the Wakeup signal within 150ms to 250ms. This value can be set optionally to 180ms, 200ms, 220ms or 240ms as it is possible accordingly with specification 2.2A. In that case, bit ERROR and bit TIMOUT are set**.** The host controller has to decide whether to transmit another Wakeup signal or not.

9.2.5.2.6 Error Detection and Handling

The LIN core generates an interrupt request and stops the processing of the current frame if it detects the following errors：

- BITMON: The bit value monitored on the bus is different from the sent bit value.
- Timeout caused by wakeup repeat timeout.
- BUS IDLE Timeout.

The errors detected in Break/Sync field will be ignored by LIN controller. The other errors happen in ID field/Data field will be recorded. In DataReq interrupt routine, the application has to check the type of error by processing the ERROR register. After that, it has to reset the ERROR register and the ERROR bit in status register by writing a 1 to bit RSTERR in control register. Starting a new message with the LIN core master or sending a Wakeup signal with master or slave is possible only if bit ERROR in status register is 0.

9.2.5.3 Auto Addressing (Lin Switch Mode):

While iND83209 integrates a lin switch and two LIN interface pins, LIN_IN and LIN_OUT, connecting to LIN transceiver. Software is in charge to control the lin switch through IOCTRLA LIN control registers. When SWON is set to 1, the lin switch will connect LIN_IN and LIN_OUT. At the same time, the lin master controller will lose the connection with the lin master transceiver.

With this lin switch, iND83209 can support auto addressing function. BCM connects iND83209 in a chain by connecting LIN_IN to upstream LIN bus, and connecting LIN_OUT to downstream LIN bus, as Figure 13. At the first boot of the system, every switch is on. The following is a SNPD sequence for instance:

1. Lin Master sends a diagnostic frame (ID=3C, 8 bytes data frame) to inform the slaves that SNPD sequence is started. Then the slaves disconnect downstream LIN bus by opening the internal switch. Thus, only the first one, iND83209 1, can receive message from BCM via LIN_IN pin.
2. Lin Master sends 1st NAD configure frame with NAD=”01”. Thus “01” address is assigned to iND83209 1 at first. And then iND83209 1 close its internal LIN switch, thus iND83209 2 can receive message from LIN bus.
3. Then system can assign the second address for iND83209 2 accordingly. By analogy, all iND83209s on the chain can be assigned address.

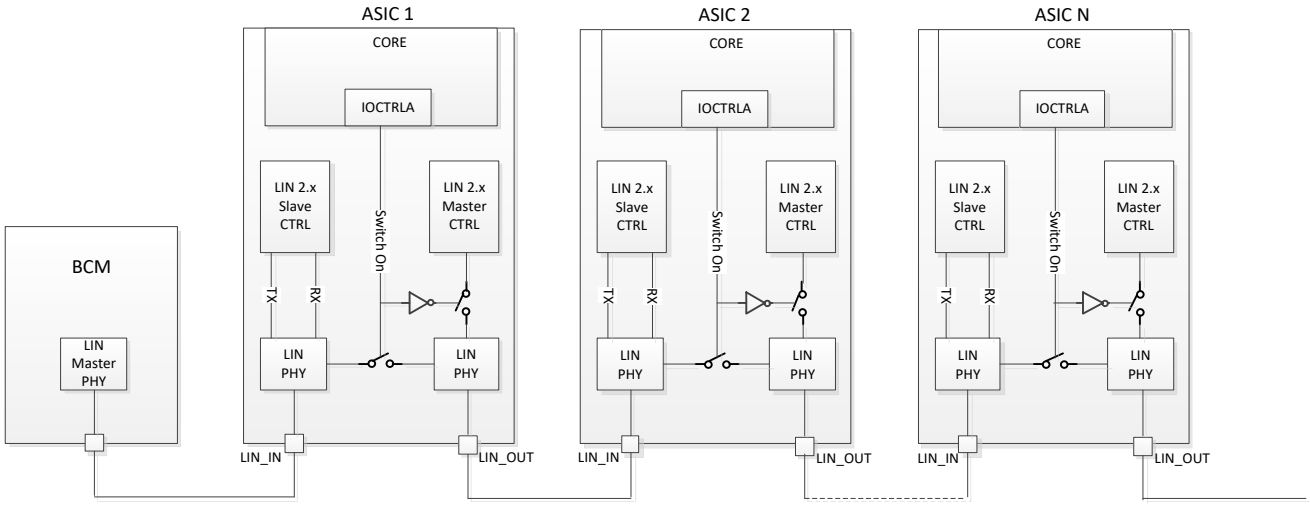


Figure 13 LIN auto addressing

Cautions:

1. LIN protocol requires inter-frame space not negative. That means any space > = 0 is acceptable. Since the internal switch is controlled by software, there are a big latency from frame complete interrupt to control the switch by interrupt routine. So a big inter-frame space is required during SNPD sequence, while this is determined by LIN master.

9.2.6 LED Driver Stage

ASIC integrates a high precision open drain LED Driver Stage that allows for LED currents in the range of 100uA to 45mA in 100uA increments. The LED bias circuit uses a precise bandgap referenced current (**CurrentV2I**) which is multiplied over stages to sink current via the LED which is connected to the HVIO(LED) pin. After factory test, the trim value for **CurrentV2I** = 30uA will be recorded and boot program is in charge of initializing the V2I trim bits correctly (refer to section 8.2.12.7 PMU_TRIM). The mirror stages consist of 100uA unit cells which are weighted linear to provide 120uA ~ 60mA current（CurrentLED）. The desired current is provided according the formula below:

$$\mathrm{CurrentLED(mA)} = \mathrm{TRIM[8:0]} * CurrentV2I * 4 = TRIM[8:0] * 120uA$$

After delicate calibration by LED trim bits(refer to section 8.2.12.11~8.2.12.13), the combination of stages allows for high accurate LED current in 120uA steps that are combined at the HVIO(LED) pad on chip (refer to Figure 14).

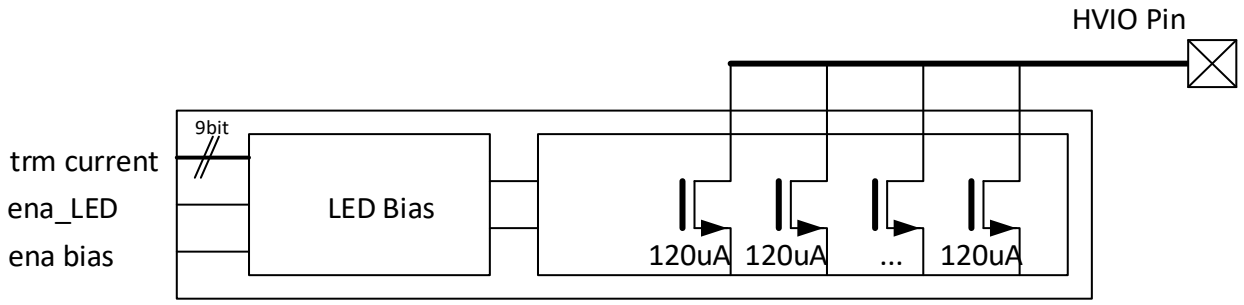


Figure 14 LED Driver Concept

The operation of the LED Driver IP requires two actions. At first the LED bias circuit needs to be enabled (ena_bias) (refer to section 8.2.12.10), followed by enabling the LED (ena_LED). Latter control signal is driven by the pulse width modulator that will drive the current from the battery via the LED. The PWM signal utilizes an input signal at maximum of 250Hz and modulates its pulse width (refer to section 9.2.7 LED PWM).

9.2.7 LED PWM

LED PWMs are used to control accurately the light intensity.

Features:

- 3x16bit PWM channels with one unified period length, independent pulse rise and pulse fall timestamps.
- Frequency and duty cycle of PWM waveform support up to a maximum Resolution of 16 bits. The 16-bit resolution is only achievable if the pre-scaler from system clock is correctly chosen to have enough clock cycles depth to count up to 2^16.
- Programmable pre-scaler: system clock division (PWM_DIV)
- Programmable PWM Period (PWM_PER)

$$\text{Period} = \frac{1 + (\text{PWM\_PER} \times \text{PWM\_DIV})}{SystemClock}$$

- Programmable duty cycle 0 to 100% (PWM_PW)

$$\text{PulseWidth} = \frac{1 + ((\text{PWM}_{\text{PFALL}} - \text{PWM}_{\text{PRISE}}) \times \text{PWM\_DIV}))}{SystemClock}$$

- Pre-scaler, period, pulse rise & pulse fall configurations will be updated at the end of the current output period.
- Support interrupt generation when new programmed PWM control data become active. After new pulse parameters (Period, pulse rise & pulse fall) have been loaded into their respective registers, an UPDATE bit can be set to 1 that will trigger the activation of the new parameters

at the end of the current pulse as not to affect the pulse shape. Basically the UPDATE bit clear is the interrupt.

- PWM Frequency range 80 - 250 Hz
- Pulse rise -> fall cases, listed in priority:
    - PRISE = 0, PFALL = PERIOD: 100% On
    - PRISE = 0, PFALL = 0: equivalent to PRISE = 0 & PFALL = 1
    - PRISE > PFALL: 100% off
    - PRISE = PFALL: 100% off
    - PRISE < PFALL: Normal case. On at PRISE, Off at PFALL.

9.2.8 House Keeping SAR ADC

- 10-bit resolution, single ended input
- Bandgap Voltage reference
- ADC is used for monitoring:
    - Band gap reference
    - Supply Voltage (limited to max voltage limited by the load dump protection circuit)
    - Differential Voltage between VBAT and HVIOs
    - Junction Temperature
    - GPIO1/2/3/4/5/6 analog input
    - VDD1V5
- ADC system capable of being configured for single or automatic multiple channel conversions (VBAT, HVIO, GPIO1~4 and Temperature Sensor).
- Interrupt on conversion complete regardless of digital comparator configuration

ADC automatic sequencer:

The following diagram shows how the VBAT (CH1), LED Forward voltage-VFW (CH2) voltages are measured along with the junction temperature monitor (CH3). VFW voltages are converted from differential voltage to single-end voltage and shifted to ADC range (1/4 attenuation). This topology guarantees excellent (VBAT-HVIO) differential voltage measurement. The DC Voltage of VBAT can also be taken but with accuracy. While both PWM and ADC sequencer run from the same system clock

(System RC Oscillator), the PWM signal is further downscaled while the ADC sampling clock can be adjusted to meet sample rate requirements. In order to reduce SW overhead, the PWM block provides a SYNC signal to the ADC sequencer which can then use this information to start the programmed conversions. In order to optimize the time taken to convert all channels (CH1,2,3) sequentially, the ADC sequencer can be configured to automatically start CHx conversion after TCURR and follow by the other channels after a duration set by TGUARD+TCHNL. TGUARD is the guard time where there is no channel selected, while switching from one channel in the sequence to the other to avoid any overlap. TCHNL is the time to wait after the guard time TGUARD for the conversions of 2nd or 3rd channel in the sequence, to allow settling of the channel before start of the conversion. The sequencer also provides a register that defines which channel need to be converted (1 to 3) and in which sequence. The sync feature is enabled by setting the SYNCENA bit and SYNCEDGE bit in ADC CNTRL Register. This enables the ADC conversion to be synchronized with the **positive edge/negative edge /period** events input which are coming from PWM outputs. In short, ADC conversion is synchronized with the event of the PWM output, if SYNCENA is set, and ADC is asked for conversion.

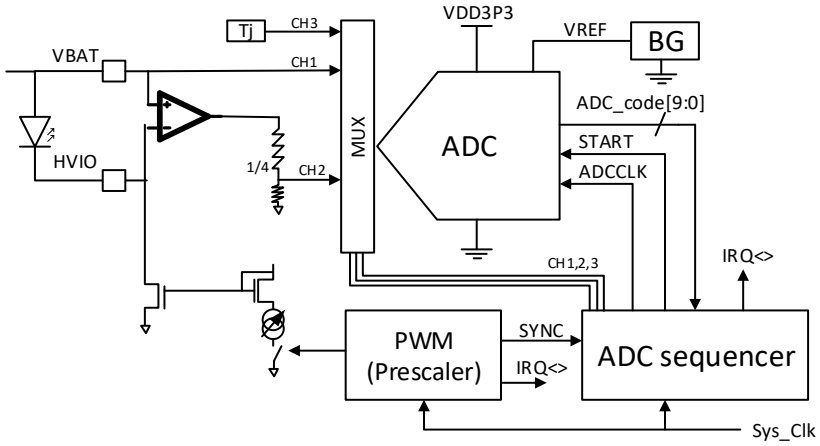


Figure 15 ADC synchronization with PWM

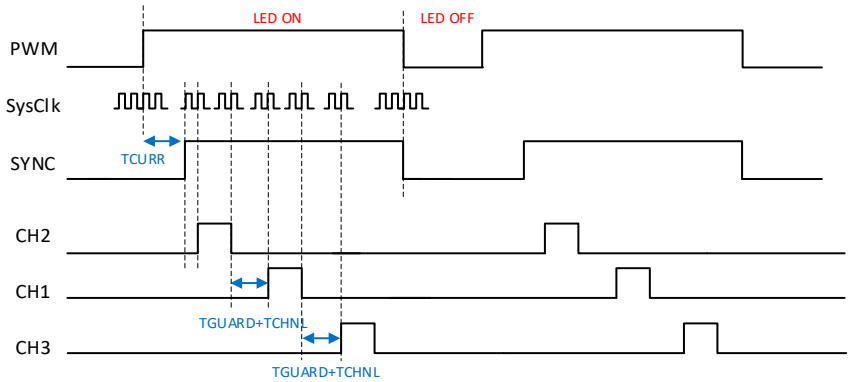


Figure 16 ADC read channels sequence triggered by PWM posedge

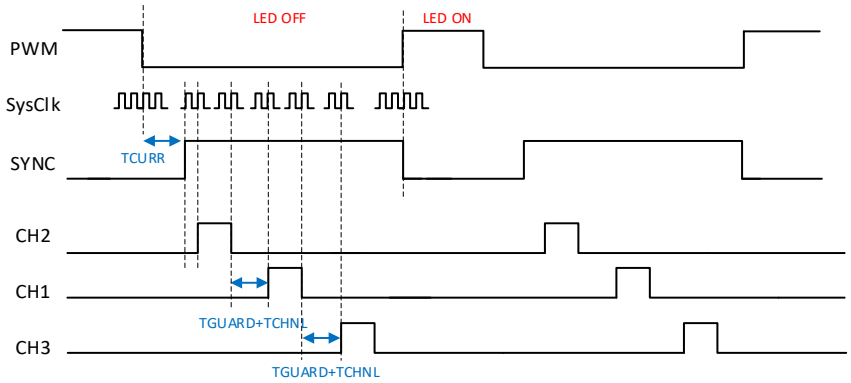


Figure 17 ADC read channels sequence triggered by PWM negedge

9.2.9 Over and Under Voltage detection (VBAT)

The over and under voltage comparators are based on comparing a divided voltage from the Load Dump limiter output feeding an analog comparator with hysteresis (refer to EC Table for electrical parameters and PMU description). The Over and Under voltage events generate Interrupts to the interrupt controller.

9.2.10 Temperature monitor

The MCU is in charge to pull the ADC related data from temperature sensor and in case the measured data is too high, MCU will reduce power profile to reduce heat. Table 16 shows the tempsensor output voltage corresponding to Tj from analog simulation for reference. Calibration is required due to different offset per chip.

Table 16 Tempsensor Output voltage vs Junction Temp

Junction Temp (°C)	Tempsensor Output Voltage(V) @VBAT=13.5V
-40	0.5125
-30	0.5345
-20	0.5565
-10	0.5785
0	0.6005
10	0.6226
20	0.6446

Junction Temp (°C)	Tempsensor Output Voltage(V) @VBAT=13.5V
30	0.6667
40	0.6887
50	0.7108
60	0.7328
70	0.7549
80	0.7770
90	0.7991
100	0.8212
110	0.8433
120	0.8654
130	0.8875
140	0.9097
150	0.9319

9.2.11 Over Temperature detection

The over temperature comparator monitors the junction temperature with hysteresis. The Over temperature event generates reset or interrupt to the interrupt controller.

9.2.12 ASIC Watchdog Timer

While it exists a watchdog timer in the MCU, the ASIC integrates another watch-dog timer that is intended to be used to recover from a situation where there may have been a software fault or other system failure where the software has ceased to operate correctly. If the timer is not reset by software periodically, it will time out, and this event can be used to reset the system or generate an interrupt (8.2.1.7 WDTACTION).

Features:

- Programmable timeout period (Refer to 8.2.6.1) with instantaneous access to the value of watchdog timeout counter
- Status flag, stop and clear/reset control registers
- The Watchdog timer is by default active after power up and set to its maximum duration setting (8.2.6.1)

- Window mode supported: If enabled, WDTA can only be cleared after the watchdog window opened and before time-out period; Otherwise, WDTA will issue a system reset or an interrupt (8.2.1.7 WDTACTION).

9.2.13 Hibernate Mode

IC must be able to enter SLEEP mode through SW request. The device should be able to come out of Hibernate with either the slow auxiliary or the system clock. It's up to the SW to select which clock shall be used after a wake event is detected. The SW should not have to request to go to Hibernate with the same clock selected for wake up.

9.2.13.1 Wake up Sources

Coming out from Hibernate mode can happen through the following events:

- After a low pulse on the LIN pin such that a dominant (low) voltage level is applied for longer than TWAKEUP time. Notice that LIN wakeup interrupts can be generated in either active or Hibernate mode when bit SLEEP = 1.
- GPIOs pin toggling either from high to low or low to high levels (VIL/VIH).
- Wake up timer. Programmable range. Wake up timer has the option to be disabled.

MCU is able to check which wake up events triggered the system through a status register read. MCU to clear the register after status check.

10 BOM

#	Description	Quantity	Comment
CBATx	2.2uF 50V X7R	1x	
CV1p5	4.7uF 10V	1x	
CV3p3	10uF 10V	1x	
DLED	Single Color LED (RGBW), TBD V	1x	OSRAM: LRTB GVSG
CLIN	220pF 0603 X7R	2x	one CLIN in master and one CLIN in slave. Only one CLIN in slave if no auto addressing is required.

11 ERRATA

11.1 ADC CONTINUOUS MODE IRQ HANDLING

The hardware implementation of continuous mode can't be trusted as it's depending on the irq subroutine execution time vs the time required to do a set sequence of conversion. For a typical interrupt handler, clear interrupt flag is required in order to allow new interrupt to be fired. But for ADC in continuous mode, the interrupts occur very intensively, new interrupt can be fired while current interrupt handling is still not yet completed, in such use cases the IRQCLR is ineffective if an new interrupt event occurs at the same time, potentially it could block any new ADC interrupt event to be fired. To avoid of such conflicts, firmware needs do additional check in the interrupt handler to make sure ADC interrupt flag is cleared successfully.

Here is an example implementation of ISR where after IRQCLR, do a check to see if there is new ADC has been done, if yes, set IRQCLR to again.

```
void ADC_Handler(void)
{
   ADC_SFRS->CNTRL.IRQCLR = 1
```

```
  while(ADC_SFRS->STATUS.CONVDONE)
    ADC_SFRS->CNTRL.IRQCLR = 1;
}
```

Alternatively, user can choose not to use ADC in continuous mode and use single conversion and setting the CONVERT every time before leaving the IRQ handler.

11.2 OVER VOLTAGE DETECTOR

If the battery voltage does transition slowly (>1mV/100ms), the OV comparator may exhibits unstable behavior with its output toggling between high and low state. The effect is eliminated by separating the thresholds for overvoltage rising and falling event (see OVLEVEL_SEL register). This can be achieved within the interrupt handler code, with the sample code written below. The different settings increase the hysteresis (still well within 18 +/-1V) and lead to single edge switching.

```
void init_ov_pol(void)
{  /* rising edit triggered */
  if(PMUA_SFRS->VBAT.HIGH)  {
    /* set falling edge voltage threshold */
    PMUA_SFRS->VBAT.OVLEVEL_SEL = 0x20;
    PMUA_SFRS->VBAT.OV_MONITOR_POL = 1;    /* flip polarity to capture falling edge */
  } else { /* falling edit triggered */
    /* set rising edge voltage  threshold back to initial SFR setting*/
    PMUA_SFRS->VBAT.OVLEVEL_SEL = 0x40;
    PMUA_SFRS->VBAT.OV_MONITOR_POL = 0;    /* for rising edge */
  }
}
```

Appendix A Slow decrease and increase of the supply voltage

(TEST-VW80000 Issue 2017-10)

Purpose

The slow decrease and increase of the supply voltage is simulated as it occurs during the slow discharging and charging processes of the vehicle battery.

Table 17 Test parameters for E-07a Slow decrease and increase of the supply voltage

Operating mode of the DUT	Operating mode " U_{Bmax} " and " U_{Bmin} " Must be performed with all relevant states of the voltage supply terminals and their combinations
Start voltage	U_{Bmax} =18V(+4%, 0%)
Rate of voltage change	0.5 V/min (+10%, -10%)
V_1	U_{Bmin} =6V
t_1	Hold time at V_1 until event memory has been completely read out
Minimum voltage	0 V
V_2	U_{Bmin} =6V
t_2	Hold time at V_2 until event memory has been completely read out
End voltage	U_{Bmax} =18V (+4%, 0%)

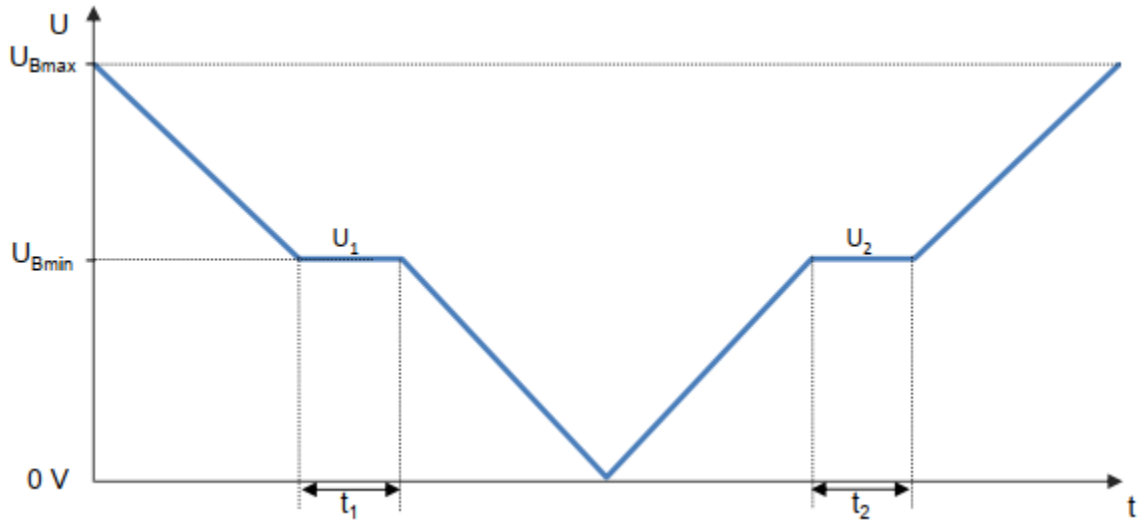


Figure 18 Test pulse for E-07a Slow decrease and increase of the supply voltage